

E-filed: 7/10/2008

IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

RAMBUS INC.,

Plaintiff,

v.

HYNIX SEMICONDUCTOR INC., HYNIX
SEMICONDUCTOR AMERICA INC.,
HYNIX SEMICONDUCTOR
MANUFACTURING AMERICA INC.,

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA,
INC., SAMSUNG SEMICONDUCTOR, INC.,
SAMSUNG AUSTIN SEMICONDUCTOR,
L.P.,

NANYA TECHNOLOGY CORPORATION,
NANYA TECHNOLOGY CORPORATION
U.S.A.,

Defendants.

No. C-05-00334 RMW

CLAIM CONSTRUCTION ORDER FOR THE
FARMWALD/HOROWITZ PATENTS AND
ORDER DENYING THE
MANUFACTURERS' MOTIONS FOR
SUMMARY JUDGMENT OF
NON-INFRINGEMENT AND INVALIDITY
DEPENDING ON CLAIM CONSTRUCTION

[Re Docket Nos. 312, 512]

RAMBUS INC.,

Plaintiff,

v.

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA,
INC., SAMSUNG SEMICONDUCTOR, INC.,
SAMSUNG AUSTIN SEMICONDUCTOR,
L.P.,

Defendants.

No. C-05-02298 RMW

[Re Docket Nos. 185, 360]

CLAIM CONSTRUCTION ORDER FOR THE FARMWALD/HOROWITZ PATENTS AND ORDER DENYING THE
MANUFACTURERS' MOTIONS FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND INVALIDITY DEPENDING
ON CLAIM CONSTRUCTION — C-05-00334 RMW; C-05-02298-RMW; C-06-00244-RMW
TSF

RAMBUS INC.,

Plaintiff,

v.

MICRON TECHNOLOGY, INC., and
MICRON SEMICONDUCTOR PRODUCTS,
INC.

Defendants.

No. C-06-00244 RMW

[Re Docket Nos. 121, 203]

Rambus has accused the Manufacturers¹ of infringing various patents. Largely in accord with the local rules, the parties have submitted their joint claim construction statement showing 72 claim terms in dispute. Rambus has filed its opening and responding *Markman*² briefs, motions for summary judgment of infringement, and oppositions to the Manufacturers' motions. The Manufacturers have filed their responsive *Markman* brief, oppositions to Rambus's summary judgment motions, and their own motions for summary judgment of invalidity under Rambus's proposed claim constructions and non-infringement under theirs. The court has reviewed the papers and considered the arguments of counsel and now sets forth its claim construction and rulings on the summary judgment motions dealing with the Farmwald/Horowitz patents. The claim construction pertaining to the Ware patents is set forth in a separate order.

I. THE FARMWALD/HOROWITZ PATENT FAMILY

Fifteen of the seventeen patents-in-suit descend from the original patent application no. 07/510,898 filed by Drs. Michael Farmwald and Mark Horowitz on April 18, 1990.³ Because these fifteen share substantially similar specifications, the court's discussion refers to U.S. Patent No.

¹ The court collectively refers to the Hynix, Micron, Nanya, and Samsung entities in this suit as "the Manufacturers."

² *Markman v. Westview Instruments, Inc.*, 517 U.S. 370 (1996).

³ The table in Appendix 1 reflects the patents-in-suit, the claims asserted, and the Manufacturers against whom the claims are asserted.

6,182,184.⁴ Given the number of claim terms in dispute and complexity of the technology, the court begins by explaining the context of the invention and the contents of the specification relevant to the disputed issues. *Cf. Phillips v. AWH Corp.*, 415 F.3d 1303, 1313, 1315-17 (Fed. Cir. 2005) (en banc). It then briefly recounts aspects of the prosecution history before turning to claim construction.

A. Background of the Inventions and the Specification's Written Description

Drs. Farmwald and Horowitz began their collaboration in the fall of 1988. Tr. 4078:21-4079:7.⁵ Dr. Farmwald met with Dr. Horowitz over dinner to discuss how processor speeds and memory speeds were diverging and how memory systems needed to become faster to keep up. Tr. 4079:9-4082:9. Within the semiconductor industry, this problem was commonly referred to as the "memory bottleneck" or "memory gap." Tr. 4084:7-4091:8 (Dr. Horowitz); 4161:10-4163:3 (Carl Everett); 5498:9-5502:8 (Dr. Farmwald). Over the course of the next year and a half, Drs. Farmwald and Horowitz worked on a variety of ideas for closing the memory gap, and they eventually wrote up their ideas in a patent application. Tr. 4133:15-4134:14. Dr. Horowitz testified that he "took over" the drafting of the specification. *Id.* The following discussion walks through the patents' common specification to illustrate the scope of the written description and explain the technology.

1. The Prior Art and Objects of the Invention

Dr. Horowitz testified that with the specification, he and Dr. Farmwald were "trying to describe our inventions, all the innovations that we had come up with to build a very high speed interface." Tr. 4134:10-14. The court will summarize here, however, only the intrinsic evidence and not the inventors' self-serving testimony. The specification begins with the field of the

⁴ Rambus's opening and reply briefs exclusively refer to U.S. Patent No. 6,426,916. The court cannot ascertain any substantive difference between the two patents' specifications. Because of the patents' different prosecution histories described at the beginning of the specification, however, citations to one patent's specification do not map to the other. Unexplainedly, the parties did not harmonize their briefing on this point.

⁵ This case has spawned a number of transcripts. Unless otherwise noted, citations to the transcript refer to the trial transcript from the bifurcated, consolidated trial the court held from January to March of 2008 regarding some of the Manufacturers' fraud and antitrust counterclaims.

1 invention, where it describes "an integrated circuit bus interface" as well as "a new method for
2 physically implementing the bus architecture." '184 patent, col. 1, ll. 21-26. From these
3 introductory sentences, it is clear that the Farmwald/Horowitz specification discloses more than one
4 invention.

5 The background of the invention discusses general features of prior art memory devices,
6 focusing on how prior art bus architectures were not as efficient as they could be. *Id.*, col. 1, l. 30-
7 col. 2, l. 5. The comparison with the prior art is extensive and illustrates some of the problems that
8 Drs. Farmwald and Horowitz sought to address with their inventions. It starts by noting that "prior
9 art memory systems have attempted to solve the problems of high speed access to memory with
10 limited success." *Id.*, col. 2, ll. 8-10. The first piece of prior art examined by the specification is
11 "the earliest 4-bit micro processor." *Id.*, col. 2, ll. 10-11 (citing U.S. Pat. No. 3,821,715 (Hoff et.
12 al.)). The Hoff micro processor connected multiple memory devices to a single CPU over a 4-bit
13 wide bus that multiplexed, i.e., carried both, address and control information. *Id.*, col. 2, ll. 13-16.
14 It also used point-to-point control signals to select which memory device the CPU sought to access.
15 *Id.* Drs. Farmwald and Horowitz critiqued aspects of the Hoff micro processor, noting that it used
16 fixed access times for transmitting information and did not permit the memory devices to send
17 information in blocks. *Id.*, col. 2, ll. 16-20. "Most important[ly]," its use of point-to-point device
18 select lines meant that it did not send device control information over the bus. *Id.*

19 The next piece of prior art discussed is U.S. Patent No. 4,315,308 (Jackson), which described
20 a bus architecture using a single 16-bit wide bus that multiplexed data, address, and control
21 information. *Id.*, col. 2, ll. 21-24. It implemented some block-mode operations and allowed some
22 access time variation, but it could not handle multiple requests and did not bus all signals. *Id.*, col.
23 2, ll. 24-30. Another patent described a DRAM with multiplexed address and data information
24 inside the DRAM, but with a "conventional" bus comprised of separate data, address, and control
25 lines to connect to the external device environment. *Id.*, col. 2, ll. 31-34.

26 Shifting away from describing prior art bus architectures, Drs. Farmwald and Horowitz
27 described prior art packaging technology. *Id.*, col. 2, ll. 35-42. While others had attempted to use 3-

1 D packages for DRAMS with connections along a single edge only, the need for point-to-point
2 wiring to enable a master device to select the correct memory device posed complex geometrical
3 problems. *Id.* No prior art packaging solution had considered using a new interface to do away with
4 the need for point-to-point device select wiring.

5 Leaving DRAM packaging and returning to DRAM architecture, Drs. Farmwald and
6 Horowitz discussed the "state-of-the-art DRAM interface" in U.S. Patent No. 3,969,706 (Proebsting,
7 et. al.). This DRAM architecture used two-way multiplexed address signals and maintained separate
8 pins for data and control information. *Id.*, col. 2, ll. 43-47. One of its problems was that it required
9 more and more pins as the DRAM grew, and many of these pins had to be connected point-to-point
10 to various devices. *Id.*, col. 2, ll. 47-50. As previously discussed, this interface complexity made
11 using a 3-D package difficult.

12 The specification next discusses backplane buses, i.e., the circuit boards used for connecting
13 multiple devices to each other. Some prior art backplane buses had multiplexed address and data
14 information, others used relatively low-voltage signals, and some others used programmable
15 registers and block mode operations. *Id.*, col. 2, ll. 51-60. While all backplane buses used some
16 arbitration scheme for prioritizing signals, none used the bus arbitration scheme devised by Drs.
17 Farmwald and Horowitz. *Id.*, col. 2, l. 61 - col. 3, l. 2. Furthermore, all prior art buses used some
18 point-to-point connections. *Id.*, col. 3, ll. 2-4.

19 Finally, the specification summarizes some prior art related to clocking a DRAM interface.
20 *Id.*, col. 3, ll. 8-21. Drs. Farmwald and Horowitz noted that "the clocking scheme used in this
21 invention has not been used before and in fact would be difficult to implement in backplane buses
22 due to the signal degradation caused by connector stubs." *Id.*, col. 3, ll. 8-11. While a prior art
23 patent had described a clocking scheme using two clock signals, it relied on unusual ramp-shaped
24 clocking signals in lieu of the conventional square signals used by Drs. Farmwald and Horowitz.
25 *Id.*, col. 3, ll. 11-14.

26 After having surveyed various aspects of the prior art, the specification sets out seven
27 "objects of the invention." *See id.*, col. 3, ll. 22-48. First, the invention uses "a new bus interface

built into semiconductor devices to support high-speed access to large blocks of data from a single memory device by an external user of the data, such as a microprocessor, in an efficient and cost-effective manner." *Id.*, col. 3, ll. 22-26. Though the invention seeks to address six other objectives, Rambus acknowledges that the "primary object that's accomplish by the claims at issue is the very first one, which is the new bus interface built into semiconductor devices to support high-speed access to large blocks of data from a single memory device." Claim Construction Hrg. Tr. 114:7-20 (June 4, 2008). The invention's second objective is "to provide a clocking scheme to permit high speed clock signals to be sent along the bus with minimal clock skew between devices." *Id.*, col. 3, ll. 27-29. The invention also seeks to provide a method for mapping out defective devices, distinguishing identical devices connected to the bus, and assigning unique identifiers to otherwise-identical devices. *Id.*, col. 3, ll. 30-35. Yet another object of the invention is to allow a device to transfer address, data, and control information over a relatively narrow bus and provide a bus arbitration scheme to allow multiple devices to use the bus simultaneously. *Id.*, col. 3, ll. 36-40. Finally, the invention seeks "to provide devices, especially DRAMs, suitable for use within the bus architecture of this invention." *Id.*, col. 3, ll. 46-48.

2. The Summary of Invention

The summary of invention begins by describing the new bus interface with substantially fewer bus lines, multiplexed address, data and control information, and no point-to-point device select lines because device select information is included in the control signal. *Id.*, col. 3, ll. 51-61. This new bus also includes clock signals and power along with the multiplexed address, data and control signals. *Id.*, col. 4, ll. 1-2. While the preferred implementation of the bus interface uses 8 bus data lines and an Addressvalid bus line, "persons skilled in the art will recognize that 16 bus data lines or other numbers of bus data lines can be used to implement the teaching of this invention." *Id.*, col. 4, ll. 5-8. With the new interface, memory devices can use the bus more efficiently by making large block data transfers and simultaneous transactions. *Id.*, col. 4, ll. 10-20.

The summary next notes that the DRAMs that connect to the new bus differ from conventional DRAMs. The new DRAMs use registers to store control information, device

information, and whatever else might be appropriate. *Id.*, col. 4, ll. 21-26. They also require circuitry for creating an internal device clock to synchronize the devices on the bus. *Id.*, col. 4, ll. 31-33.

Finally, the summary of invention explains that the constrained bus environment enables high clock speeds by shortening the necessary length of the bus. *Id.*, col. 4, ll. 35-50. Taken as a whole, these innovations improve DRAM bandwidth while reducing manufacturing costs and power consumption. *Id.*, col. 4, ll. 51-55.

3. The Detailed Description

The detailed description of the invention begins with an overview of the new technology, then splits into discrete sections addressing various features of the invention. These feature-specific discussions address: device address mapping (col. 7, l. 17), bus (col. 8, l. 16), protocol and bus operation (col. 8, l. 42), retry format (col. 12, l. 1), system configuration/reset (col. 14, l. 46), error detection and correction (col. 16, l. 20), low-power 3-D packaging (col. 17, l. 14), bus electrical description (col. 17, l. 62), clocking (col. 18, l. 62), multiple buses (col. 19, l. 45), device interface (col. 21, l. 23), electrical interface—input/output circuitry (col. 21, l. 41) and DRAM column access modification (col. 23, l. 42). Only some of these discussions bear on the construction and validity of the claims in dispute.

a. The Multiplexed Bus Architecture

The detailed description starts by noting that "the present invention is designed to provide a high speed, multiplexing bus for communication between processing devices and memory devices and to provide devices adapted for use in the bus system." *Id.*, col. 5, ll. 29-31. The bus has a number of features. First, it is narrow, i.e., it has a relatively small number of bus lines. *Id.*, col. 5, ll. 35-37. Second, it is multiplexed, meaning, it carries substantially all address, data and control information on the same bus data lines. *Id.*, col. 5, ll. 37-45. This obviates the need for device-select lines because device-select information is carried over the bus. *Id.*

The devices connected by the bus include master devices like the CPU and slave devices like a DRAM. *Id.*, col. 6, ll. 12-16. Every semiconductor device, whether master or slave, has a number

1 of programmable registers for storing information, including device identification, device type, and
 2 control settings. *Id.*, col. 6, ll. 27-52. For example, preferred embodiments of the patent's
 3 semiconductor devices contain access-time registers that store delay times that control when the
 4 device can send and receive data. *Id.*, col. 6, ll. 32-37. These register settings can be modified when
 5 the device is turned on. *Id.*, col. 6, ll. 38-52.

6 The specification's preferred bus architecture has 11 signal lines. *Id.*, col. 8, ll. 17-34. There
 7 are eight bus data lines referred to as "BusData0" through "BusData7" and collectively described as
 8 BusData[0:7]. *Id.*, col. 8, ll. 17-23. These data lines provide a multiplexed bus for address, data and
 9 control information that is one byte wide. *Id.*, col. 8, ll. 24-25. There are also two clock lines (Clk1
 10 and Clk2) and an AddrValid line. *Id.* These lines serve to synchronize all of the devices on the bus
 11 and to indicate whether the information on the bus includes an address request for all slave devices
 12 to decode. *Id.*, col. 8, ll. 25-30. Finally, there is an additional line (ResetIn, ResetOut) that connects
 13 all devices attached to the bus. While the other signal lines on the bus connect to every device in
 14 parallel, the ResetIn, ResetOut line connects all of the devices in series so that it can program their
 15 registers and assign them unique device identification numbers. *Id.*, col. 8, ll. 30-35.

16 **b. The Packet Protocol**

17 The bus is the sole courier of information between devices on the bus. *Id.*, col. 6, ll. 53-55.
 18 This requires a communication protocol. *Id.*, col. 6, ll. 55-60. The specification describes using a
 19 packet protocol. *Id.* It begins when a master device sends a request packet ("a sequence of bytes
 20 comprising address and control information"). *Id.* Every slave device must decode the packet to
 21 determine if it must respond to the request packet. *Id.*, col. 6, ll. 62-64. If it does, the slave device
 22 begins its internal processes and responds to the request packet by sending or retrieving data after a
 23 programmed delay time. *Id.*, col. 6, l. 64 - col. 7, l. 4.

24 A preferred embodiment of the protocol begins when a master device sends out a request
 25 packet of address and control information onto the bus. *Id.*, col. 8, ll. 59-62. The AddrValid line is
 26 activated, which instructs all slave devices to decode the incoming request packet and decide
 27 whether the request packet applies to them. *Id.*, col. 8, l. 66 - col. 9, l. 4. If the packet contains the

slave device's address, the slave device responds by either transmitting data to the master for a read request or receiving data from the master for a write request. *Id.* This response occurs after a delay time specified in the memory device's access-time register. *Id.*, col. 9, ll. 11-23.

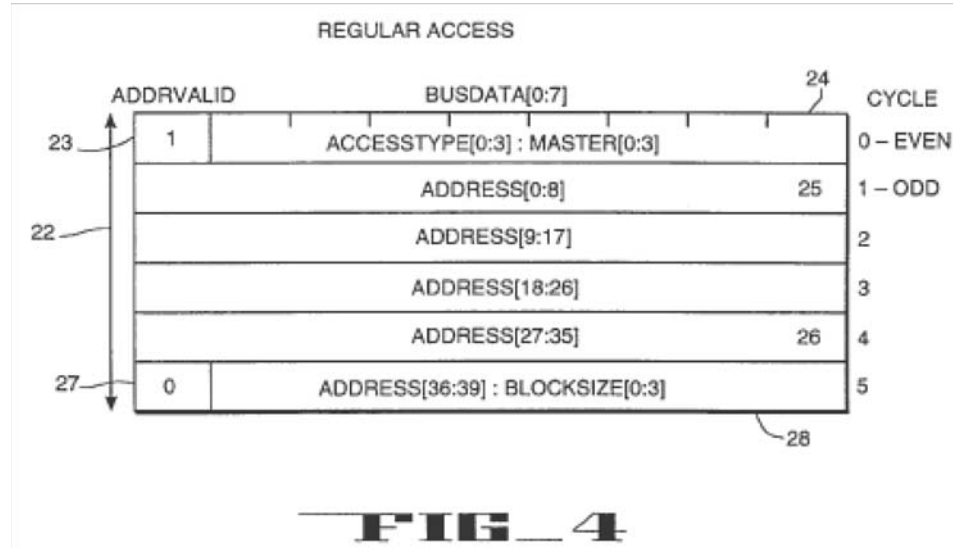


Figure 4 shows the preferred embodiment of a request packet. The request packet is nine bits wide, corresponding to the AddrValid bus line plus the eight bus data lines BusData[0:7], and the packet is six bytes long. *Id.*, col. 9, ll. 24-29. The first byte begins with the AddrValid bit equal to 1 to indicate the beginning of a request packet. *Id.*, col. 9, ll. 29-31. The first byte then contains two four-bit fields sent over the bus data lines. *Id.*, col. 9, ll. 39-46. The first four bits are known as AccessType[0:3]. *Id.*, col. 9, ll. 39-41. AccessType[0:3] is an "op code" or "operation code" that specifies the type of access for the DRAM to perform. *Id.* The second four bits, known as Master[0:3], serve to identify the master device sending the request packet. *Id.*, col. 9, ll. 41-46. Briefly, the forty bits of address data in Address[0:35] and Address[36:39] specify the slave device that should perform the requested operation. *See id.*, col. 9, ll. 35-38. Finally, the last four bits of the request packet, known as BlockSize[0:3], tell the DRAM the amount of data involved in the requested operation. No actual data is sent or received in the request packet. The request packet simply allows each DRAM on the bus to: (1) recognize the next six bytes as a request packet, (2) understand what operation is requested, (3) recognize the source of the request packet, (4) determine whether the request packet is addressed to it, and (5) determine the amount of data to send or receive

1 in response to the request packet.

2 In the preferred embodiment, AccessType[0], i.e., the first bit of the four bit AccessType[0:3]
3 field, is a read/write switch. *Id.*, col. 9, ll. 47-56. If AccessType[0] equals 1, the requested operation
4 is a read and the DRAM should access the data in its memory array and output the data to the bus.
5 *Id.*, col. 9, ll. 50-56. If AccessType[0] equals zero, the requested operation is a write and the DRAM
6 should prepare to receive data from the bus. *Id.* The other three bits of the AccessType field,
7 AccessType[1:3], could be used to specify the delay time of the DRAM's response or trigger
8 preprogrammed responses. *See id.*, col. 9, ll. 56-65; col. 11, ll. 19-37. For example, AccessType[3]
9 can be used to tell the DRAM whether to precharge the sense amplifiers in the memory device to an
10 intermediate voltage between zero and one to allow for a faster response to the next request or to
11 save the information already contained in the memory array. *See id.*, col. 10, ll. 15-48; col. 11, l. 37.

12 The BlockSize[0:3] field determines the size of the following data block transfer. *Id.*, col.
13 11, ll. 38-39. In the preferred embodiment, if BlockSize[0] equals zero, the size of the following
14 data block corresponds to the binary value of BlockSize[1:3], enabling the data block to be 0 to 7
15 bits long. *Id.*, col. 11, ll. 39-40. If BlockSize[0] equals one, the data block's length corresponds to
16 the value of 2 to the power of the binary value of BlockSize[1:3], beginning with 2³, or 8, bits in
17 length. *Id.*, col. 11, ll. 40-41. Hence, a BlockSize[0:3] equal to 0001 corresponds to a data block
18 that is one bit long. By contrast, a BlockSize[0:3] equal to 1111 corresponds to a data block that is
19 1,024 bits long, i.e., 2¹⁰. *See id.*, col. 11, ll. 48-57. These interpretations of BlockSize[0:3] are only
20 illustrative; other encoding schemes are possible simply by changing the meaning of the field's
21 values.

22 Once the DRAM has decoded the request packet, it must wait the programmed delay time.
23 *Id.*, col. 11, ll. 61-63. It then responds by reading or writing data over the bus lines BusData[0:7] while
24 the AddrValid bus line remains set to zero to indicate that data, and not another request packet, are
25 being transmitted on the bus. *Id.*

26 c. The Clocking Scheme – External and Internal Clock Signals

27 As a memory device gets faster, i.e., as the time between signals decreases (or, as the

frequency of the system increases), the time a signal takes to propagate down the bus becomes significant compared to the time between signals. This error created by the time it takes for the signal to travel can disrupt the ability of the memory devices to operate synchronously with each other.

The specification discloses one way of minimizing this error by having each device receive two clock signals. *Id.*, col. 18, ll. 63-66. The device can then use the two external clock signals to derive an internal device clock. *Id.* If every device uses the external clock signals to derive the same internal clock signal, each device's internal clock can reflect a true system clock shared by all devices, despite the devices being in different positions on the bus. *Id.*

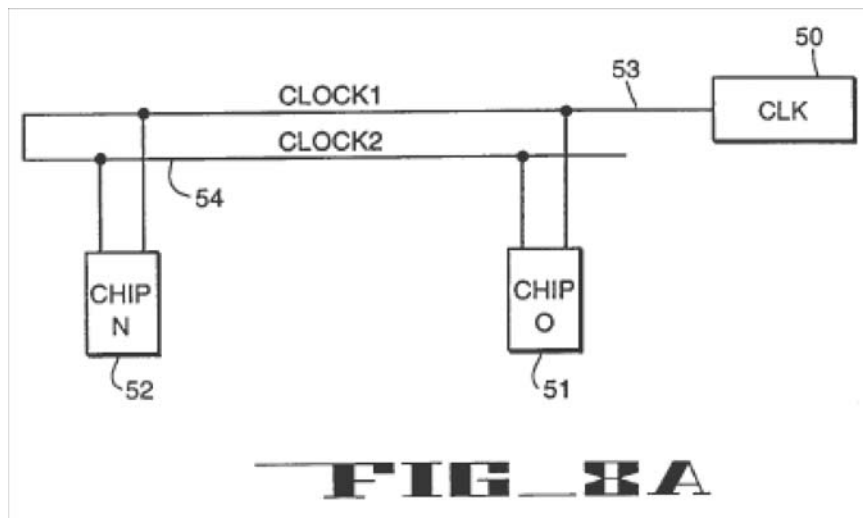


Figure 8a shows the preferred embodiment of the clocking scheme devised by Drs. Farmwald and Horowitz. The clock generator (CLK) sends an early clock signal along the bus's CLOCK1 line, where the signal first contacts Chip O and later contacts Chip N. *Id.*, col. 19, ll. 3-7. The clock signal then loops around on a second line (the CLOCK2 bus line), where it now contacts Chip N first, then contacts Chip O. *Id.*, col. 19, ll. 7-10. An alternative embodiment uses only one bus clock line and leaves the end of the clock line unterminated, allowing the clock signal to reflect back when it reaches the end of the clock line. *Id.*, col. 19, ll. 10-13. The reflected clock signal performs the same function as the CLOCK2 signal in the preferred embodiment while remaining confined to the same clock line. *Id.*

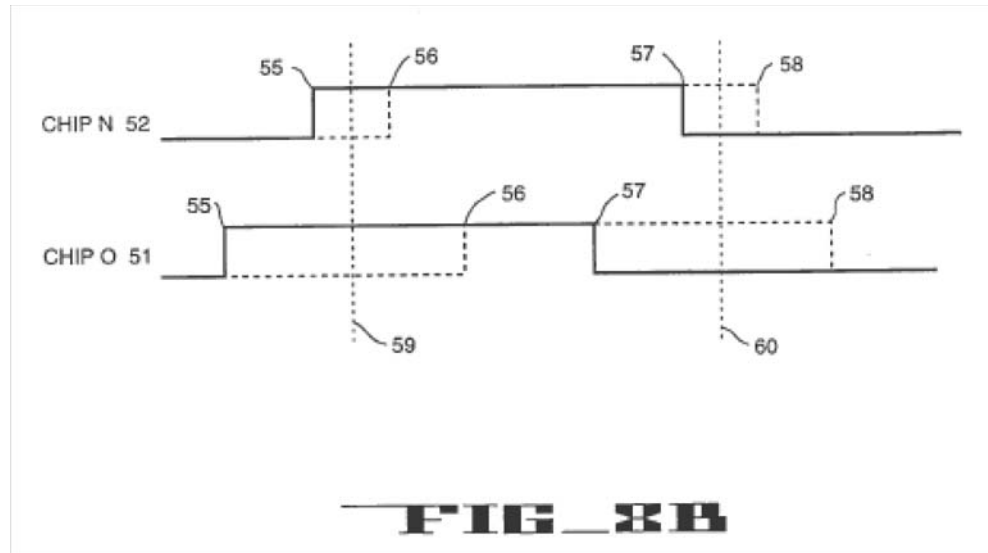


Figure 8b depicts the method used by each memory device to derive an internal clock signal from the two external clock signals.⁶ Figure 8a's example shows that Chip O is closer to the clock generator. Chip O therefore receives the clock signal on CLOCK1 before Chip N, as demonstrated by comparing when each chip detects an increase in voltage on CLOCK1 (represented by the solid black line, 55). *See id.*, col. 9, ll. 14-32. Meanwhile, Chip N is closer to the source of CLOCK2 than Chip O. Therefore, Chip N receives the second clock signal, CLOCK2, earlier than Chip O. *Id.* CLOCK2 is shown in Figure 8b by the dashed line, 56.

If each memory device is connected to the bus's clock signal lines properly, the *average* of the times at which each chip receives CLOCK1 and CLOCK2 should be identical. In Figure 8b, this is shown as the dashed vertical line labeled 59. Thus, despite the propagation delay caused by each device being placed at a different point on the bus, each device can use two external clock signals to derive an internal clock signal that is the same in every device.

Figure 8b demonstrates another feature of Drs. Farmwald and Horowitz's invention, namely, the use of both edges of the clock signal (also referred to as the rising and falling edges of the clock signal) to gain twice the amount of information out of a single period of the clock signal. *See id.*,

⁶ Figure 8b lacks axis labels on its two graphs. To a person of ordinary skill in the art, it would be clear that the x-axis represents time. It would be similarly clear that the y-axis represents the voltage on the clock lines, as measured by each chip.

col. 9, ll. 33-44. As discussed, the two chips on the bus use the transition of the two clock signals from low to high to derive the midpoint depicted by the dashed line 59. The two chips also detect when each clock signal decreases, i.e., goes from high to low, as shown at 57 (CLOCK1) and 58 (CLOCK2). Each chip can calculate the midpoint of the two decreases in the two clock signals, shown by the dashed vertical line 60. As with the prior midpoint, the two chips are connected to the clock signal lines so that the midpoint measured by Chip N is the same as the midpoint measured by Chip O. By using the midpoint of the rise and fall of the two clock signals, the devices on the bus can respond at two different points in time for each period of the clock signal. Thus, the bus data frequency can be twice the clock signal frequency. *See id.*

d. The Clocking Scheme – Responding to Internal Clock Signals

The preceding discussion omits some of the complex details required to compensate for the lag between the internal clock signal and the device's interaction with the other bus lines. To begin, a device requires both input and output circuitry for responding to signals from the bus. The input circuitry includes an "input sampler" for measuring the voltage on the bus lines and detecting an incoming signal. *See id.*, col. 22, ll. 21-35. The output circuitry contains an "output driver" for putting data onto the bus. *See id.*, col. 22, ll. 1-20. For example, the input sampler has a slight delay between when it receives a clock signal and its sampling of the bus's data lines. Because of the system's high frequency, it is important to minimize any such delay. *Id.*, col. 22, ll. 50-56.

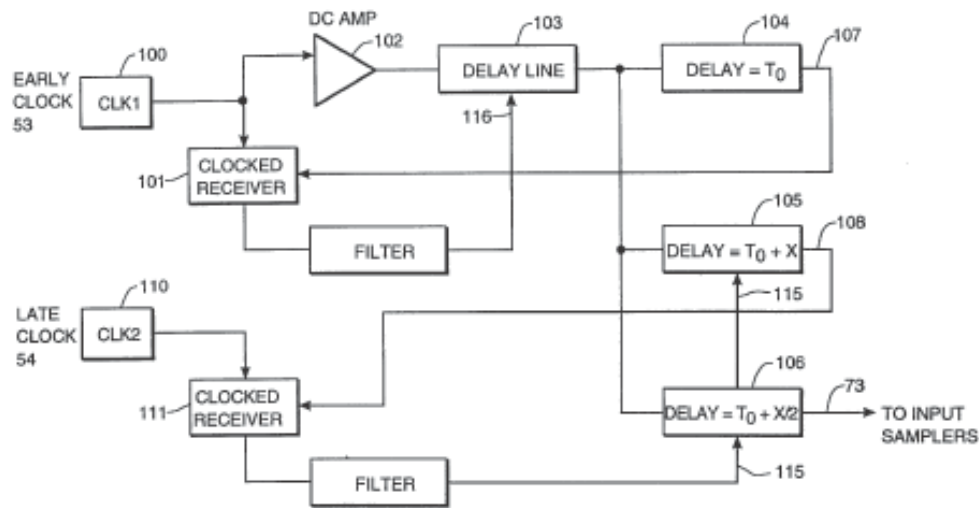
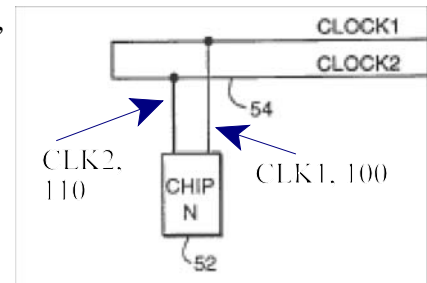
FIG. 12

Figure 12 reveals that omitted complexity. The first thing to recognize is the inputs for the first clock signal (early clock, or CLOCK1) and second clock signal (late clock, or CLOCK2). The connections between the device and the bus's clock lines are labeled CLK1 (100) and CLK2 (110). To help orient Figure 12 within the context of the prior discussion, the edited excerpt of Figure 8a below needs to be referenced. All of the circuitry shown in Figure 12 exists in each device attached to the bus.

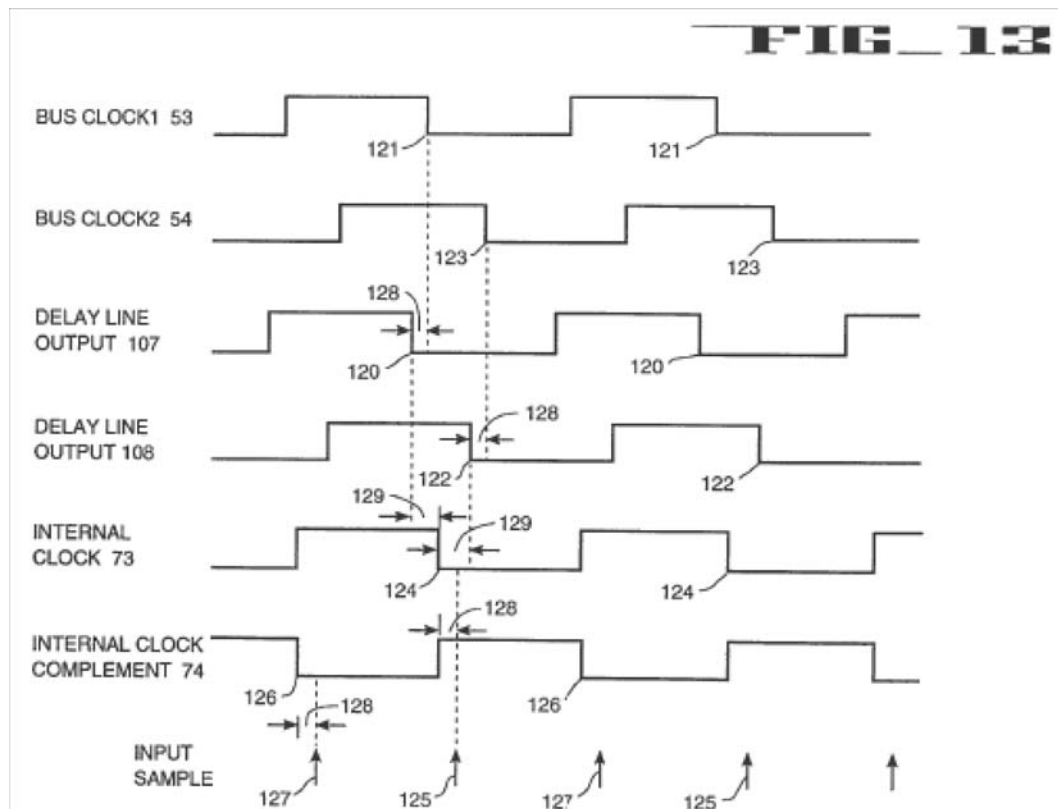
The first element of the circuit is a DC amplifier (102), which is necessary for converting the bus clock line's relatively low voltage signal into a more powerful signal that the device can more readily recognize. *See id.*, col. 22, ll. 60-61. The amplified clock signal then feeds into a variable



delay line (103), which in turn feeds three different delay lines (104, 105, and 106). *Id.*, col. 22, ll. 61-66. The first delay line (104) has a fixed delay time. *Id.* The second delay line (105) has the same fixed delay time plus a second variable delay time. *Id.* The third delay line (106) has the same fixed delay as the prior two lines plus a variable delay time that is half of delay line 105's second variable delay time. *Id.* In Figure 12, the fixed delay time is represented as T_0 and the second

variable time is represented as X. The third delay line's delay time equals the midpoint of the delay times of the first and second delay lines.

The outputs of the first two delay lines (104 and 105) are labeled 107 and 108. *Id.*, col. 22, ll. 66-67. These outputs connect to the clocked input receivers on each of the two bus clock lines labeled as 101 and 111. *Id.*, col. 22, l. 66 - col. 23, l. 4. To be clear, these input receivers receive *two* signals: the external clock signal from the bus's clock line and the internal delay signal. *See id.*, col. 23, ll. 2-4 & Fig. 11. The clocked receivers then run feedback lines (115, 116) back into the variable delay lines (103, 105). *Id.*, col. 23, ll. 3-7. The timing diagram in Figure 13 assists in understanding the purpose of all of this circuitry.



As with Figure 8b, the unlabeled x-axis is time and the unlabeled y-axes of the graphs in Figure 13 are the voltage levels on the various lines. For context, labels 121 and 123 correspond to the falling edges of the first and second, or early and late, bus clocks. *Id.*, col. 23, ll. 7-13. When properly calibrated, delay lines 107 and 108 output signals similar to the early and late bus clocks respectively, but shifted early by a slight amount (128). *Id.*, col. 23, ll. 3-13. This slight amount

(128) is ideally equal to the delay time before the input sampler can respond to the clock signal and sample the bus's data lines. *Id.*

As discussed, the third delay line has a fixed delay time and half of the variable delay time of the second delay line. This puts the output of the third delay line (also known as the internal clock signal 73) at the midpoint of the other two delay lines. *Id.*, col. 23, ll. 13-18. This is simply the distance labeled 129 between the internal clock signal's falling edge (73) and the two internal delay lines' falling edges (labeled 120 and 122). This final output is the device's derived internal clock signal, which precedes the true midpoint of the two bus clocks by a small amount of time equal to the delay in the input sampler's operation. In the preferred embodiment, the device also generates an inverse of the internal clock signal, referred to as the complementary internal clock signal and labeled 74 in Figure 13.

To complete the story, the device has two internal clock signals that mirror each other. Each precedes the true midpoint of the bus clock signals by an amount of time equal to the delay in operating the input sampler. The preferred embodiment then harnesses half of the input samplers to one clock signal and has them sample the bus on the clock signal's falling edge, while the other half of the input samplers sample the bus on the complement's falling edge. *Id.*, col. 23, ll. 26-34. In such a fashion, the device successfully samples the bus for data at the midpoint of the two external clock signals' rising and falling edges.

B. Prosecution History

1. The Original 11-Way Restriction Requirement

As mentioned, Drs. Farmwald and Horowitz filed their original patent application no. 07/510,898 with 150 claims on April 18, 1990. The PTO responded with a restriction requirement, forcing Drs. Farmwald and Horowitz to separate their claims into 11 distinct applications. *See Detre Decl.*, Ex. A. The examiner defined a first group of claims (Group I, covering claims 1-45 and 56-72) as the combination of "a memory and bus subsystem including address registers, transceivers, and memory sections" and a "general mention of memory control." *Id.* at 3. He then proceeded to distinguish other groups of claims as follows:

CLAIM CONSTRUCTION ORDER FOR THE FARMWALD/HOROWITZ PATENTS AND ORDER DENYING THE MANUFACTURERS' MOTIONS FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND INVALIDITY DEPENDING ON CLAIM CONSTRUCTION — C-05-00334 RMW; C-05-02298-RMW; C-06-00244-RMW

Group	Original claims	Basis for distinction	Source
II	46-55	Group I related to memory control generally. Group II claims "a specific memory control and arbitration scheme."	<i>Id.</i> at 3.
III	73-81	Group I related to timing generally. Group III claims "a specific clocking and timing scheme."	<i>Id.</i> at 4.
IV	82-90	Group IV claimed "an unrelated DRAM device."	<i>Id.</i> at 1.
V	91-94	Group V claimed "an unrelated semiconductor package."	<i>Id.</i> at 1.
VI	95-105	Group VI claimed "a semiconductor device and connection means" and generally mentioned "bus characteristics." The examiner did not find a "combination/subcombination" relationship between Group I and Group VI.	<i>See id.</i> at 4-5.
VII	106, 107	Group VI made only "a general mention of bus characteristics." Group VII claimed "specific bus characteristics."	<i>Id.</i> at 5.
VIII	108-110	Group VI generally mentioned "timing and clocking." Group VIII included "specific clocking and timing considerations."	<i>Id.</i> at 6.
IX	111-113	Group VI generally mentioned "storage." Group IX included "specific receiving and storage means."	<i>Id.</i> at 6.
X	114-123	Group VI generally mentioned "I/O." Group X related to "a specific I/O and multiplexing scheme."	<i>Id.</i> at 7.
XI	124-150	Group VI generally mentioned "input and output." Group XI related to "a specific input/output scheme using packets."	<i>Id.</i> at 8.

In laying out the details of the original restriction requirement, the court recognizes its limited evidentiary significance. First, the examiner purportedly distinguished claims going to separate inventions. This clearly distinguished groups IV and V from the other inventions. What is unclear is the relationship, if any, between Group I and Group VI. The examiner used the same shorthand to refer to both groups as the combination A and subcombination B_{br}, jointly "AB_{br}." Yet he defined the meaning of "A" differently for Group I and Group VI. For Group I, "A" represented "a memory and bus subsystem including address registers, transceivers, and memory sections." For Group VI, "A" represented "a semiconductor device and connection means." Because it appears that Group I and Group VI claim different inventions, it seems that the additional prosecution history of each is of little relevance to the other.

Second, the examiner divided claims to a combination and a subcombination into distinct

groups where (1) "the combination as claimed does not require the particulars of the subcombination as claimed for patentability" and (2) the subcombination has utility by itself. *See, e.g., id.* at 3. This is how the examiner distinguished groups II and III from group I and groups VII through XI from group VI. The examiner found the first requirement met whenever the subcombination's details appeared in a dependent claim. *See id.* Because all of the claims were *assumed* to be patentable, the presence of the subcombination in a dependent claim was evidence that the combination did not require the subcombination for the combination to be patentable. *See id.* To be clear, the examiner's restriction is *not* evidence that each separate group is supported by the specification and separately patentable. It is only evidence that the claims, as drafted, were directed at separate inventions. *Accord Honeywell Int'l., Inc. v. ITT Industries, Inc.*, 452 F.3d 1312, 1319 (Fed. Cir. 2006) (assigning little weight to restriction requirement that did not construe claim terms or consider the specification).

2. Additional Restrictions

All of the patents-in-suit (and the vast majority of the Farmwald/Horowitz patent family) descend from Group I. Group I's prosecution history is rife with additional restrictions. One in particular is worth noting. On June 5, 1997, the examiner issued a restriction requirement for application no. 08/798,520 distinguishing claims to "a semiconductor device having at least one access-time register" and claims to "a memory device having a plurality of conductors being multiplexed for sequentially receiving an address." The examiner noted that the two groups of claims do not require each other and would require separate prior art searches. In response, Rambus elected to proceed with the claims to a semiconductor device with an access-time register.

II. PRIOR CLAIM CONSTRUCTION ORDERS

The Farmwald/Horowitz family of patents have been previously construed in various cases involving Rambus. Certain claim terms – "integrated circuit device," "read request," "write request," "transaction request" and "bus" – have been construed by the Federal Circuit. *Rambus Inc. v. Infineon Techs. AG*, 318 F.3d 1081, 1089-95 (Fed. Cir. 2003). This court construed additional terms in a previous case between Rambus and Hynix. *Hynix Semiconductor Inc. v. Rambus Inc.*, C-

00-20905-RMW, 2004 WL 2610012 (N.D. Cal. Nov. 15, 2004) (*Hynix I*). The Manufacturers acknowledge these prior decisions, but argue about the amount of deference owed to them.

A. *Stare Decisis* and the *Infineon* Decision

In *Markman v. Westview Instruments, Inc.*, the Supreme Court cited with approval authority that treated claim construction as a question of law, not fact, and held that claim construction is exclusively the responsibility of the court. 517 U.S. 370 (1996). The issue for the Court was whether the Seventh Amendment requires a jury to construe a patent. *See id.* at 372. Because history and precedent provided no clear answer, the Court examined "functional considerations" to determine the scope of the Seventh Amendment's right to a jury trial *See id.* at 388. The Court held that a judge, not a jury, would be better suited to interpret a patent as a written document, in part because jurors remain "unburdened by training in exegesis." *Id.* at 388-89. The Court also noted that a jury's ability to evaluate testimony would not be as helpful as a judge's ability to parse a complex document. *Id.* at 389-90.

The *Markman* Court buttressed its holding that functional considerations compel assigning claim construction to the court by emphasizing the "importance of uniformity in the treatment of a given patent." *Id.* at 390. The Court pointed out that issue preclusion cannot impose uniformity on infringement defendants who were not a party to a prior action. *Id.* at 391 (citing *Blonder-Tongue Laboratories, Inc. v. University of Ill. Foundation*, 402 U.S. 313 (1971)). After noting the difficulty of ensuring uniformity through issue preclusion, the Court stated that "treating interpretive issues as purely legal will promote (though it will not guarantee) intrajurisdictional certainty through the application of *stare decisis* on those questions not yet subject to interjurisdictional uniformity under the authority of the single appeals court." *Id.*

Since *Markman*, courts have treated this discussion as granting *stare decisis* effect to the Federal Circuit's claim constructions. *E.g.*, *Key Pharmaceuticals v. Hercon Laboratories Corp.*, 161 F.3d 709, 716 (Fed. Cir. 1998) ("We do not take our task lightly in this regard, as we recognize the national *stare decisis* effect that this court's decisions on claim construction have."); *Hynix I*, 2004 WL 2610012, at *4; *Wang Laboratories, Inc. v. Oki Electric Industry Co., Ltd.*, 15 F. Supp. 2d 166,

1 176 (D. Mass. 1998). A district court must apply the Federal Circuit's claim construction even
 2 where a non-party to the initial litigation would like to present new arguments. *E.g., Wang*
 3 *Laboratories*, 15 F. Supp. 2d at 176 (applying the Federal Circuit's prior claim construction to a non-
 4 party whose motion to intervene as *amicus* at the Federal Circuit had been denied). Here Hynix,
 5 Micron, Nanya, and Samsung – none of whom were parties to the *Infineon* proceedings⁷ – ask this
 6 court to deviate from the Federal Circuit's claim construction in *Infineon*.

7 The Manufacturers do not dispute that *stare decisis* applies to a claim construction order
 8 generally. Instead, the Manufacturers suggest that a court may depart from binding precedent where
 9 the legal basis for the prior ruling has been sufficiently eroded. The Manufacturers quote the First
 10 Circuit for the principle that "*stare decisis* is neither a straightjacket nor an immutable rule; it leaves
 11 room for courts to balance their respect for precedent against insights gleaned from new
 12 developments, and to make informed judgments as to whether earlier decisions retain preclusive
 13 force." *Carpenters Local Union No. 26 v. U.S. Fidelity & Guar. Co.*, 215 F.3d 136, 142 (1st Cir.
 14 2000). The Manufacturers argue that the Federal Circuit's recent cases on claim construction have
 15 altered the inquiry so much that this court should not follow *Infineon*. In urging this court to "not
 16 follow outdated decisions," the Manufacturers overlook a fundamental principle of *stare decisis*:
 17 only the court that issued the decision in question can elect not to follow it. *See State Oil Co. v.*
 18 *Khan*, 522 U.S. 3, 20 (1997) ("[I]t is this Court's prerogative alone to overrule one of its
 19 precedents."). The Federal Circuit recently illustrated this deference in *Independent Ink, Inc. v.*
 20 *Illinois Tool Works, Inc.*, a case where the criticism of the existing precedent was overwhelming.
 21 *See* 396 F.3d 1342, 1349-51 (Fed. Cir. 2005), *rev'd by Illinois Tool Works Inc. v. Independent Ink,*
 22 *Inc.*, 547 U.S. 28 (2006). Nonetheless, the Federal Circuit abided by "the duty of a court of appeals
 23 to follow the precedents of the Supreme Court until the Court itself chooses to expressly overrule
 24 them." *Id.* at 1351. This duty applies with equal force to this court and its relationship to the

25
 26 ⁷ Hynix and Micron did submit an *amicus* brief in support of panel rehearing or rehearing
 27 *en banc* regarding the portion of the *Infineon* decision dealing with fraud. *See Rambus Inc. v. Infineon*
Techs. AG, 2003 WL 24027551 (Fed. Cir. Mar. 7, 2003). This brief did not address the claim
 28 construction issues in the *Infineon* decision.

Federal Circuit.

The Manufacturers argue that the *Phillips* case has so altered claim construction that the Federal Circuit would have decided *Infineon* differently had it heard the case today. The court does not read *Phillips* as working so great a change. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1330 (Fed. Cir. 2005) (Mayer, J., dissenting) ("Again today we vainly attempt to establish standards by which this court will interpret claims. But after proposing no fewer than seven questions, . . . we say nothing new, but merely restate what has become the practice over the last ten years."). Nonetheless, it cannot entertain that question because *Phillips* did not overrule *Infineon* or change the rules of claim construction such that *Infineon*'s constructions need to be revisited. Accordingly, the court adopts the Federal Circuit's construction of "integrated circuit device," "read request," "write request," "transaction request" and "bus" from *Infineon*. For ease of reference, the court reproduces these constructions below:

Claim term	Construction	Citation
"integrated circuit device"	A circuit constructed on a single monolithic substrate, commonly called a 'chip.'	318 F.3d at 1091.
"read request"	A series of bits used to request a read of data from a memory device where the request identifies what type of read to perform.	<i>Id.</i> at 1093.
"write request"	A series of bits used to request a write of data to a memory device.	<i>Id.</i> at 1093.
"transaction request"	A series of bits used to request performance of a transaction with a memory device.	<i>Id.</i> at 1093.
"bus"	A set of signal lines to which a number of devices are connected, and over which information is transferred between devices.	<i>Id.</i> at 1095.

In applying the *Infineon* claim construction, the court is sensitive to the fact that three of the Manufacturers have never been heard on this subject. Their arguments seeking to interpret terms in the claims such that the alleged inventions are limited to use with the inventors' narrow, multiplexed bus architecture has appeal, and if the court were construing the claim language on a clean slate, it might well so limit the claims. However, the slate is not clean. The Federal Circuit reviewed the intrinsic evidence and concluded that "[a]lthough some of Rambus's claimed inventions require a

1 multiplexing bus, multiplexing is not a requirement in all of Rambus's claims." *Infineon*, 318 F.3d at
 2 1094. This court cannot, no matter how appealing, contradict the *Infineon* claim construction.

3 **B. *Stare Decisis* and the *Hynix I* Decision**

4 The parties next dispute how much deference this court owes to its prior claim construction
 5 in the earlier *Hynix* proceedings. The *Markman* Court commented that treating claim construction
 6 as a matter of law would "promote (though it will not guarantee) intrajurisdictional certainty through
 7 the application of *stare decisis* on those questions not yet subject to interjurisdictional uniformity
 8 under the authority of the single appeals court." 517 U.S. at 391. The Court's reference to
 9 promoting, but not guaranteeing, "intrajurisdictional certainty" suggests that a district court should
 10 follow another court's claim construction, though it does not have to.

11 Since *Markman*, various district courts have taken slightly different approaches to other
 12 courts' claim constructions, but despite the Court's suggestion, none has applied *stare decisis*. One
 13 court held that "considerable deference should be given to those prior decisions unless overruled or
 14 undermined by subsequent legal developments, including intervening case law." *Sears Petroleum &*
 15 *Transport Corp. v. Archer Daniels Midland Co.*, 2007 WL 2156251, at *8 (N.D.N.Y. 2007). It then
 16 proceeded to consider arguments that it had not heard during the prior claim construction. *Id.* at
 17 *12. Similarly, another court held that it would defer to its prior claim construction, but only "to the
 18 extent the parties do not raise new arguments." *KX Industries, L.P. v. PUR Water Purification*
 19 *Products, Inc.*, 108 F. Supp. 2d 380, 387 (D. Del. 2000). Another court feared that refusing to
 20 consider a new party's claim construction arguments raised due process concerns and therefore
 21 granted the party's request for a *Markman* hearing. *Texas Instruments, Inc. v. Linear Technologies*
 22 *Corp.*, 182 F. Supp. 2d 580, 589-90 (E.D. Tex. 2002). Meanwhile, courts in this district have been
 23 willing to consider a prior claim construction, but have stressed the importance of conducting an
 24 independent inquiry. *Visto Corp. v. Sprogit Techs., Inc.*, 445 F. Supp. 2d 1104, 1108-09 (N.D. Cal.
 25 2006) (Chen, M.J.); *see also Townshend Intellectual Property, L.L.C. v. Broadcom Corp.*, 2008 WL
 26 171039 (N.D. Cal. Jan. 18, 2008) (Fogel, J.) (modifying prior claim construction in light of a new
 27 party's arguments).

This general practice accords with the insight that a fresh look at a claim construction can hone a prior court's understanding and construction of a patent. *See e.g., Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1329 (Fed. Cir. 2008). Indeed, the Federal Circuit has said that it "would be remiss to overlook another district court's construction of the same claim terms in the same patent as part of [a] separate appeal." *Id.* In *Finisar*, the Federal Circuit found a second district court's claim interpretation particularly helpful where it referred back to the prior construction and noted where it disagreed. *Id.* The lesson from *Finisar* is that additional litigation can refine and sharpen the courts' understanding of an invention and that a second court should *not* defer to a prior court's claim construction without questioning its accuracy.

On the other hand, this practice appears to conflict with the Supreme Court's understanding of *stare decisis*. The Supreme Court has stated that "[c]onsiderations in favor of *stare decisis* are at their acme in cases involving property and contract rights, where reliance interests are involved." *Payne v. Tennessee*, 501 U.S. 808, 828 (1991). As early as 1851, the Supreme Court explained in dictum that "*stare decisis* is the safe and established rule of judicial policy, and should always be adhered to" when dealing with cases establishing rules of property. *The Genessee Chief*, 53 U.S. 443, 458 (1851). The Court applied similar thinking in *Minnesota Mining Co. v. National Mining Co.*, 70 U.S. 332 (1865), to reject a repeated attempt to litigate the possession of an estate. The Court reasoned that rules of property engender reliance, and that changing such rules damages any interests that have grown up based on those rules. *Id.* at 334. Contemplating the issue of mistaken decisions, the Court mused that "[d]oubtful questions on subjects of this nature, when once decided, should be considered no longer doubtful or subject to change." *Id.* Such firmness would discourage parties from "speculat[ing] on a change of the law" and free the courts from "the infliction of repeated arguments by obstinate litigants, challenging the justice of [the court's] well-considered and solemn judgments." *Id.*

"*Stare decisis* is usually the wise policy, because in most matters it is more important that the applicable rule of law be settled than that it be settled right." *Burnet v. Coronado Oil & Gas Co.*, 285 U.S. 393, 406 (1932) (Brandeis, J., dissenting). However, the prevailing notion among the

1 district courts and the *Finisar* court is that it is better to get a claim construction right than it is to get
2 a claim construction settled. Why so many courts have intuitively reached this conclusion is not
3 immediately clear. It may stem, however, from the imperfect analogy between a patent right and
4 other property rights, or from the difficulty of construing complex technical terms without the
5 benefit of the arguments of parties not involved at the time of the first construction. In explaining
6 when to apply *stare decisis*, Justice Brandeis stressed that it should apply "even where the error is a
7 matter of serious concern, provided correction can be had by legislation." *Burnet*, 285 U.S. at 406.
8 Unlike a common law rule of contract or property, a patent interpretation cannot be readily narrowed
9 by a statute. It is doubtful Congress would take the time to do such a thing, and doing so could raise
10 Fifth Amendment concerns. When approaching *stare decisis* from the perspective of what
11 institution could best fix a mistaken interpretation, a court rather than the legislature is probably in a
12 better position to do so.

13 The Supreme Court has emphasized that "legislatures may alter or change their laws, without
14 injury, as they affect the future only; but where courts vacillate and overrule their own decisions on
15 the construction of statutes affecting the title to real property, their decisions are retrospective and
16 may affect titles purchased on the faith of their stability." *Minnesota Mining Co.*, 70 U.S. at 334.
17 This basis for *stare decisis* reflects concerns about society's reliance on a rule of law and the harm
18 associated with upsetting society's expectations. *See Payne*, 501 U.S. at 828 (modulating the impact
19 of *stare decisis* based on the weight of reliance interests). It is unclear how many people develop
20 reliance interests in any given claim construction. At its grandest, a claim construction could shape
21 an entire industry's research and development efforts (by leading people to avoid research in an area
22 already patented) and licensing relationships (by leading people to take licenses or buy a favorably
23 construed patent), as well as various company's stock prices (the patent holder's could increase on a
24 favorable claim construction while an infringing firm's might collapse). But this is rather
25 speculative, and even at its greatest, a claim construction does not engender the same scope of
26 reliance on property rights that animated the Court's holding in *United States v. Title Insurance &*
27 *Trust*, 265 U.S. 472 (1924), where a reversal would have redistributed huge tracts of land overnight.

1 While a change in the scope of a patent may dry up a royalty stream, it would not lead to ejectments
2 and repossessions.⁸

3 Thus, while "most" matters benefit from being settled rather than being settled right, claim
4 construction appears to be an exception, at least as among district courts. Further, since the
5 constructions in *Hynix I* are not final, the court is free to revisit them. Accordingly, this court will
6 initially treat its prior construction as correct, but consider the Manufacturers' arguments as to why a
7 construction in *Hynix I* should be modified.

8 C. Collateral Estoppel as to Hynix

9 Putting aside Micron, Nanya, and Samsung, Rambus argues that Hynix should be precluded
10 from challenging the court's prior claim construction. Preclusion does not attach lightly. As stated
11 by the Ninth Circuit, a court's decision only bars relitigation of an issue where:

- 12 (1) the issue necessarily decided at the previous proceeding is identical to the one
13 which is sought to be relitigated;
14 (2) the first proceeding ended with a final judgment on the merits; and
15 (3) the party against whom collateral estoppel is asserted was a party or in privity
16 with a party at the first proceeding.

17 *Hydranautics v. FilmTec Corp.*, 204 F.3d 880, 885 (9th Cir. 2000); *see also Kourtis v. Cameron*, 419
18 F.3d 989 (9th Cir. 2005).

19 Rambus points out that a court has precluded a party from relitigating claim construction in
20 situations where there appears to have not been a final judgment. *E.g., TM Patents, L.P. v. Int'l Bus.*
21 *Machines Corp.*, 72 F. Supp. 2d 370, 376-80 (S.D.N.Y. 1999). The prior action in *TM Patents*
22 ended during trial when the parties settled. *Id.* at 375. Nonetheless, the court in the second action
23 precluded TM Patents from relitigating the prior court's claim construction because it held that the
24 decision was sufficiently "final." *Id.* at 375-76 (citing *Lummus Co. v. Commonwealth Oil Ref. Co.*,
25 297 F.2d 80, 89 (2d Cir. 1961)). Indeed, the law of issue preclusion uses an unusual definition of

26 ⁸ Reliance interests could be harmed if a patent was narrowly construed, industries
27 developed, and then a later court broadened a claim to cover those investments. While this is a concern
28 in patent law, *see, e.g., Miller v. Bridgeport Brass Co.*, 104 U.S. 350 (1881), it does not apply here. A
patent holder that suffered a narrow claim construction might appeal that claim construction, but would
likely be estopped in the future from attempting to broaden its claims.

"final judgment," namely, any adjudication that is "sufficiently firm" to be accorded preclusive effect. *Luben Industries, Inc. v. United States*, 707 F.2d 1037, 1040 (9th Cir. 1983); *see also* Rest. 2d of Judgments § 13.

Still, the court is unpersuaded that its *Hynix I* claim construction order is "sufficiently firm" to grant it preclusive effect. There has not yet been a final judgment in the earlier proceedings, preventing Hynix from obtaining appellate review of this court's claim construction. The inability to obtain appellate review bars the application of issue preclusion. *Matter of Lockard*, 884 F.2d 1171, 1176 (9th Cir. 1989) (citing Rest. 2d of Judgment § 28(1)). While the claim construction in *TM Patents* also could not be appealed, that was caused by the patentee's decision to settle, not because the law prevented appellate review. *See* Rest. 2d of Judgments § 28, cmt. a (noting that 28(1) "applies only when review is precluded as a matter of law. It does not apply in cases where review is available but is not sought."). Because Hynix has not yet been able to exercise its right to appeal this court's prior claim construction, it cannot be precluded from continuing to litigate the scope of Rambus's patent claims.

III. CLAIM CONSTRUCTION

The parties dispute the construction of a number of terms and so focused their arguments on groups of terms. After briefly addressing the claim construction legal standard, the court's inquiry follows the parties' groupings of the disputes.

A. Claim Construction Legal Standard

The court begins its claim construction inquiry by considering the ordinary and customary meaning of the terms in the claims from the perspective of a person of ordinary skill in the art. *Phillips*, 415 F.3d at 1312-13. This ordinary meaning is influenced by the use of language in the asserted and unasserted claims in the patents. *Id.* at 1314-15. For example, the phrase "steel baffles" implies that a "baffle" need not be made of steel. *See id.* at 1314. More generally, the appearance of a limitation in a dependent claim creates a presumption that the independent claim lacks that limitation. *Id.* at 1315; *but see Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1380-81 (Fed. Cir. 2006) (discussing limits of claim differentiation).

1 This "objective baseline" of ordinary meaning is also formed in part by the patents'
2 specification's use of the claim language because a person of ordinary skill understands a claim's
3 language in the context of the entire patent. *Id.* at 1313. For example, the specification is often
4 helpful in defining the scope of technical terms. *See id.* at 1315. The specification can also reveal a
5 "special definition" of a claim term or demonstrate "an intentional disclaimer" or "disavowal" of
6 claim scope. *Id.* at 1316. The specification's statutory role in determining a claim's validity justifies
7 placing this heavy weight on it. *Id.* at 1315-16.

8 Similarly, the prosecution history of a patent can inform the proper construction of a patent's
9 claims. *Id.* at 1317. It provides evidence of how both the Patent Office and the inventor understood
10 the claims. *Id.* The prosecution history's back-and-forth nature often makes it unclear, however, and
11 therefore it is rarely as helpful in construing a patent's claims as the claims themselves and the
12 specification. *Id.* Still, the prosecution history can be invaluable for demonstrating the inventor's
13 understanding of the claims and checking "whether the inventor limited the invention in the course
14 of prosecution, making the claim scope narrower than it would otherwise be." *Id.*

15 Finally, a court may consider extrinsic evidence like inventor and expert testimony,
16 dictionaries, and treatises. *Id.* at 1318. Such evidence can be helpful, but courts must be mindful
17 that it is not necessarily created contemporaneously with the patent application and that the litigation
18 context can produce biased evidence. *Id.* Accordingly, extrinsic evidence is rarely more probative
19 of the proper construction of the claims than the intrinsic record, *id.* at 1319, but extrinsic evidence
20 is particularly helpful "[w]hen the intrinsic evidence is silent as to the plain meaning of a term."
21 *Helmsderfer v. Bobrick Washroom Equipment, Inc.*, 527 F.3d 1379, 1381-83 (Fed. Cir. 2008)
22 (construing a claim term in light of three dictionary definitions); *see also Phillips*, 415 F.3d at 1322-
23 23. Nonetheless, to avoid "the risk of systematic overbreadth" the court begins its inquiry focused
24 "on how the patentee used the claim term in the claims, specification, and prosecution history, rather
25 than starting with a broad definition and whittling it down." *Phillips*, 415 F.3d at 1321.

26 All four sources of evidence discussed above have their advantages and drawbacks and
27 varying amounts of persuasive force. All of the sources are appropriately considered, and contrary

to Samsung's argument at the claim construction hearing, there is no "rigid algorithm" or "sequence of steps" which the court must follow. *Id.* at 1324. All that matters "is for the court to attach the appropriate weight to be assigned to those sources in light of the statutes and policies that inform patent law." *Id.*

B. The "Device" Terms and Multiplexing

The first dispute between the parties is whether Rambus's claims should be limited to DRAMs that use multiplexed bus data lines. This dispute touches on the construction of "bus" from *Infineon* and influences the construction of "device" and variants of "device." Rambus argues that there is no need to construe the term "device" in isolation, but that the court should adopt the *Infineon* court's construction of "integrated circuit device" and the construction of "memory device" from *Hynix I*. The Manufacturers proffer a detailed and limited construction of the term "device," which they then incorporate into their proposed constructions of "integrated circuit device" and "memory device." The proposed constructions appear below:

Claim term:	Rambus's construction:	The Manufacturers' Construction:
"device"	(no separate construction)	Electronic circuits or components with a bus interface that is adapted to connect to a multiplexed set of signal lines, each for carrying address, data, and control information, that has substantially fewer connections to signal lines than the number of bits in a single address, and that does not connect to a separate device select line.
"integrated circuit device"	A circuit constructed on a single monolithic substrate, commonly called a "chip."	A device that includes one or more integrated circuits.
"memory device"	An integrated circuit device in which information can be stored and retrieved electronically.	A device in which information can be stored and retrieved electronically.

1. "Device"

At bottom, the Manufacturers' proposed construction of "device" is an attempt to evade the Federal Circuit's *Infineon* construction of the terms "integrated circuit device" and "bus." The Manufacturers' proposed construction of device, when incorporated into the phrase integrated circuit device, conflicts with the Federal Circuit's construction of that phrase, which lacks the narrow,

1 multiplexed bus limitation of the Manufacturers' proffered construction. *See Infineon*, 318 F.3d at
 2 1089-91. The Manufacturer's construction of "device" also imports a multiplexing limitation into
 3 every claim, an interpretation the Federal Circuit already considered and rejected when it construed
 4 the term "bus." *Id.* at 1094-95. The court also rejected any attempt to read a multiplexing limitation
 5 into other claim terms when it held that "multiplexing, if necessitated by the claims, is applicable to
 6 the construction of the term 'bus,' not 'read request.'" *Id.* at 1093. Hynix previously made this
 7 argument regarding the construction of "device," and the court rejected it because "[t]his end result,
 8 a multiplexed bus as part of the claim limitations, was rejected by the Federal Circuit." *Hynix I*,
 9 2004 WL 2610012, at *6.

10 The Manufacturers argue that the court should ignore the Federal Circuit's interpretation of
 11 "bus" because the claims-in-suit do not use the term. From this, the Manufacturers argue that the
 12 Federal Circuit's interpretation of "bus" should not influence the interpretation of "device" because
 13 "bus" is not in dispute.⁹ Even if the term "bus" were not in dispute here, the court cannot ignore the
 14 Federal Circuit's construction of the term because this court cannot construe a claim to blatantly
 15 conflict with the Federal Circuit's prior interpretation. *See Hynix I*, 2004 WL 2610012, at *6.

16 Nor is the court necessarily persuaded that the Manufacturers' construction of "device" is
 17 correct, even if the court could ignore the *Infineon* claim construction. The Manufacturers'
 18 construction of "device" would import a host of limitations, specifically that the device (1) be
 19 adapted to connect to a multiplexed set of signal lines, (2) have substantially fewer connections to
 20 signal lines than the number of bits in a single address, and (3) lack a separate device select line.
 21 That a person of ordinary skill in the art would read the term "device" and necessarily understand the
 22 term to have all of these limitations is questionable.

23 The court does note that the specification is dense with discussion of the advantages of the
 24 multiplexed bus architecture at the heart of Drs. Farmwald and Horowitz's invention. The most

25
 26 ⁹ Rambus requests that the court construe "bus," and construe it in light of *Infineon*,
 27 because the term appears in the Manufacturers' proposed constructions. Hence, while the claims do not
 28 recite the term "bus," the term has been put in dispute by the Manufacturers' use of the term in their
 proposed constructions.

1 compelling piece of evidence presented by the Manufacturers is that the detailed description of the
2 invention begins with "the present invention is designed to provide a high speed, multiplexing bus
3 for communication between processing devices and memory devices and to provide devices adapted
4 for use in the bus system." '184 patent, col. 5, ll. 29-31. Furthermore, the specification's defined
5 objectives include "provid[ing] devices, especially DRAMs, suitable for use with the bus
6 architecture of the invention." *Id.*, col. 3, ll. 46-48. The Manufacturers therefore argue that the
7 specification necessarily limits the claimed devices to ones "adapted for use in the bus system."

8 But these modifications do not all *require* the multiplexed bus architecture. For example,
9 programmable registers can contain device identification information, device-type information, and
10 access-time settings, among other things. *See id.*, col. 6, ll. 28-37. To be sure, a register for device
11 information is unnecessary where the bus architecture uses device-select lines. However, nothing
12 about the use of an access-time register hinges on the use of a multiplexed bus architecture. While
13 using programmable delay times is useful in the multiplexed bus environment, it is not limited to
14 that environment. This fact is reflected in the prosecution history. As discussed above, at one
15 juncture the examiner required Rambus to split its claims because the use of access-time registers
16 did not require a multiplexed bus, and vice versa. *Accord Infineon*, 318 F.3d at 1095. To construe
17 "device" to require the use of a multiplexed bus (among other things) would run counter to the
18 Patent Office and the inventors' disclosed understandings of the claims.

19 2. "Integrated circuit device"

20 Putting aside the dispute over multiplexing, the Manufacturers argue that an "integrated
21 circuit device" should be construed to include "one or more integrated circuits," while Rambus
22 argues that the court should adopt the Federal Circuit's narrower *Infineon* construction that limited
23 an "integrated circuit device" to a circuit built on a single chip.

24 It is unclear why this claim construction dispute must be resolved. The joint case
25 management order in this case set a deadline for filing summary judgment motions that depend on
26 claim construction issues. *See* C-05-00334-RMW, Docket No. 174, at Attachment C (N.D. Cal.
27 Apr. 24, 2007). The Manufacturers have moved for summary judgment of non-infringement based

1 on the court's adoption of their various claim constructions, and have also moved for summary
2 judgment of invalidity based on the court's adoption of Rambus's proposed claim constructions.
3 However, the Manufacturers' bring no motion that adoption of any of *their* proposed claim
4 constructions would compel summary judgment of invalidity.

5 This prevents the court from fully grasping the nature of the claim construction dispute. For
6 example, the Manufacturers' motion suggests that construing the term "device" to include a
7 multiplexing limitation might support a summary judgment of non-infringement. But their motion
8 does not advance a non-infringement argument based on the "one or more chips" construction of
9 "integrated circuit device." Indeed, it would be hard to imagine how requesting a broader claim
10 construction than that of the patent holder could lead to a finding of non-infringement. This leaves
11 the court to speculate as to why this dispute is material. Either this dispute is about nothing, or the
12 Manufacturers are suggesting that the court construe a claim so broadly that it is invalid. This
13 uncertainty defeats the purpose of the court's case management order.

14 That aside, the court begins with the Federal Circuit's claim construction from *Infineon*
15 holding that an integrated circuit device is limited to a single chip. In reaching its decision, the
16 Federal Circuit considered the lower court's claim construction, Rambus's position, and the ordinary
17 meaning of the term "integrated circuit" based on two computing dictionaries. *See Infineon*, 318
18 F.3d at 1091. The Manufacturers now argue that while the Federal Circuit construed an "integrated
19 circuit device" as being limited to a single chip, it did not explicitly consider whether the claim must
20 be limited to a single chip or could encompass multiple devices. The Manufacturers are correct;
21 Infineon does not appear to have argued that an "integrated circuit device" could be more than one
22 integrated circuit. Instead, it argued that an "integrated circuit device" had to contain three types of
23 circuitry based on Rambus's specification. *See Infineon*, 318 F.3d at 1089-90. Rambus meanwhile
24 advocated its view of the ordinary meaning of the phrase.

25 The Manufacturers also point out that the Federal Circuit relied on definitions of integrated
26 circuit, while Rambus's claims refer to an integrated circuit *device*. The Manufacturers argue that
27 adding "device" means the phrase is broader than just one integrated circuit, and therefore the phrase

should be construed as comprising one or more integrated circuits. The Manufacturers also identify an instance in the prosecution history of Rambus's claims where it referred to "a single semiconductor substrate" and argue that this distinction shows that an "integrated circuit device" is broader than a single chip. In reply, Rambus characterizes the Manufacturers' construction as "absurdly broad" such that "many modern washing machines would be 'integrated circuit devices.'" Rambus also argues that the Manufacturers do not explain why "integrated circuit device" should be construed more broadly than "integrated circuit." On the other hand, Rambus does not credibly explain why "integrated circuit device" should *not* be construed more broadly than "integrated circuit." Nor does Rambus point to anything in the claim language, specification, or prosecution history to support its argument that an "integrated circuit device" must necessarily exist on a single chip.

While the Manufacturers' argument has some appeal, the court is bound by the claim construction in *Infineon*. *Stare decisis* would be largely meaningless if a lower court could change an appellate court's interpretation of the law based only on a new argument. Here, the Federal Circuit has definitively interpreted the phrase "integrated circuit device" in the context of the Farmwald/Horowitz patent family as "a circuit constructed on a single monolithic substrate, commonly called a 'chip.'" This court may not revisit it.

3. "Memory device"

In *Hynix I*, this court interpreted a "synchronous memory device" as "a memory device that receives an external clock signal which governs the timing of the response to a transaction request." *Hynix I*, 2004 WL 2610012, at *6-*8. The court's analysis focused on the "synchronous" aspect of the phrase and did not independently focus on the phrase "memory device." The reason is that the term "memory device" was not contested in *Hynix I* – the parties agreed that it meant "an integrated circuit device in which information can be stored and retrieved electronically." *See* C-00-20905, Docket No. 326, at 1 (N.D. Cal. Sept. 15, 2003).

Rambus emphasizes repeatedly that it is proposing the same construction that it and Hynix

1 agreed to in 2003.¹⁰ The Manufacturers propose that a "memory device" is simply "a device in
2 which information can be stored and retrieved electronically." The difference is merely whether a
3 "memory device" incorporates the definition of an "integrated circuit device," and with it, the single
4 chip limitation from *Infineon*.

5 Rambus points to a number of illustrative references to a memory device in the patents'
6 common specification. First, Rambus notes that the specification refers to DRAMs, SRAMs, and
7 ROM devices as "memory devices" and assumes that these memory devices are confined to a single
8 chip. '184 patent, col. 1, ll. 49-56. Next, Rambus shows that "one object of the present invention is
9 to use a new bus interface built into semiconductor devices to support high-speed access to large
10 blocks of data from a single memory device by an external user of the data, such as a
11 microprocessor, in an efficient and cost-effective manner." *Id.*, col. 3, ll. 23-27. It is unclear why
12 this sentence would compel a person of ordinary skill in the art to interpret a "memory device" as
13 residing on a single chip. Somewhat more helpfully, Rambus shows that in the summary of
14 invention, Rambus described the present invention as "a memory subsystem comprising at least two
15 semiconductor devices, including at least one memory device, connected in parallel to a bus"
16 *Id.*, col. 3, ll. 51-61. Another portion of the specification describes how the DRAMs claimed in the
17 patent differ from other DRAMs, namely, because they include "registers . . . which may store
18 control information, device identification, device-type and other information appropriate for the *chip*
19 such as the address range for each independent portion of the device." *Id.*, col. 4; ll. 22-27
20 (emphasis added). This sentence suggests that a DRAM must exist on a single chip, but it is not
21 clear that it requires a "memory device" to be a single chip. Rambus also refers to a paragraph of the
22 detailed description where the patent states that "the bus architecture of this invention connects
23 master or bus controller devices, such as CPUs, Direct Memory Access devices (DMAs) or Floating
24 Point Units (FPUs), and slave devices, such as DRAM, SRAM, or ROM memory devices." *Id.*, col.

25
26 ¹⁰ It must be noted that since Hynix and Rambus disagreed about the meaning of "integrated
27 circuit device," which was embedded within their definition of "memory device," the parties did not
28 really agree on the meaning of "memory device" – they only agreed that the definition turned on the
definition of "integrated circuit device."

6, ll. 12-17. The description reinforces the linkage between "memory devices" and chips like DRAMs when it states that "a memory device will typically have only slave functions, while a DMA controller, disk controller or CPU may include both slave and master functions." *Id.*, col. 6, ll. 20-23. Lastly, the patents' drawings also support Rambus's argument; for example, figure 8a shows two DRAMs attached to a bus and refers to them as "chips."

As Rambus often points out, a court must "avoid importing limitations from the specification into the claims." *Phillips*, 415 F.3d at 1323. However, where a specification clearly states the scope of an invention and the scope of the invention is "described as the advantage and distinction of the invention," the specification may narrow the ordinary scope of the claims. *E.g.*, *On Demand Machine Corp. v. Ingram Indus., Inc.*, 442 F.3d 1331, 1340 (Fed. Cir. 2006). The *On Demand* case is illustrative of how explicitly a specification must define the scope of the invention for the specification to limit the scope of the claims. For example, the patentee in *On Demand* clearly distinguished its customer-oriented book printing machine from "general purpose machines." *Id.* at 1340. From this, the Federal Circuit held that the claimed machine that enabled a customer to select a book to print on demand required a physically present consumer instead of a remote purchaser.

Rambus's references to the specification show that a DRAM, SRAM or ROM *may* be a memory device, but the specification does not clearly limit the term "memory device" to a single chip. Because the specification does not clearly limit the scope of the invention to a single chip, the court declines to read the phrase "memory device" so narrowly. Accordingly, the court adopts the Manufacturer's construction. A "memory device" is "a device in which information can be stored and retrieved electronically." It need not be on a single chip.

Similar to its arguments about the need to limit "integrated circuit device" to not read on a washing machine, Rambus argues that the Manufacturers' construction of "memory device" could cover a tape recorder because it is a "device in which information can be stored and retrieved electronically." Rambus's hyperbolic argument ignores that its claims contain more limitations than just "a memory device." Putting aside other limitations, the claims often (but not always) modify the phrase "memory device." For example, Rambus asserts claim 43 of U.S. Pat. No. 6,314,051. That

claim specifically limits itself to "[t]he memory device of claim 34 wherein the memory device is a synchronous dynamic random access memory." Rambus also asserts claims 1 and 34 of U.S. Pat. No. 6,584,037. These claims are drawn to "a method of operation of a synchronous memory device" and "a method of operation of a synchronous dynamic random access memory device." These additional limits on the scope of "memory device" ameliorate fears that Rambus's claims could read on a "tape recorder," while also demonstrating that Rambus knew how to limit its claims to a single chip when it wished to do so. *See Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1380-81 (Fed. Cir. 2007); *cf.* Mark A. Lemley, *The Limits of Claim Differentiation*, 22 Berkeley Tech. L. J. 1389, 1396 (2007).

C. The "Transaction" Terms and the Packet-Based Protocol

The next significant dispute between the parties turns on whether Rambus's claims extend to DRAMs that do not use a packet-based protocol for transmitting information. This dispute influences the construction of "read request," "write request," "operation code," "block size information," and a host of additional terms incorporating these or similar terms.

Like the dispute over the "device" terms, the "transaction" terms appear throughout Rambus's claims. Also like the "device" terms, the Federal Circuit has already construed some of the terms at issue. As these interpretations control this court's decision making, the inquiry begins with them.

1. "Read Request," "Write Request," and "Transaction Request"

Claim term:	Rambus's Construction:	The Manufacturers' Construction:
"write request"	A series of bits used to request a write of data to a memory device where the request identifies what type of write to perform.	One or more bits in a write request packet to request a write of data to a memory device, where the write request packet identifies the type of write to perform.

Rambus's construction of write request is illustrative of its constructions of "read request" and "transaction request," all of which reflect the Federal Circuit's construction of those terms. *Infineon*, 318 F.3d at 1093. The Manufacturers' construction is essentially identical, except it requires that a request be contained in a request packet.

Again, the court begins with the Federal Circuit's construction in *Infinion*. There, Infineon argued that a "read request" must also include address and control information. *Id.* The Federal Circuit characterized Rambus as arguing that "address and control information is part of the 'request packet,' not the 'read request'" and that the read request was simply "an instruction to the memory device to perform a read action." *Id.* The Federal Circuit's opinion accurately summarizes Rambus's argument then. Rambus characterized the four bits AccessType[0:3] as the "read request." *See* Brief of Plaintiff-Appellant Rambus Inc., *Rambus Inc. v. Infineon Techs. AG*, 2001 WL 34773495, *17 (Fed. Cir. Nov. 6, 2001) ("Specifically, the 'read request' consists of 4 digital 'bits,' called the AccessType field, which are contained within the larger 'request packet,' as shown in Fig. 4."). So there can be no mistake, Rambus's brief repeated that "a 'read request' (and, correspondingly, a 'write request') is determined by and consists of the AccessType field, 4 digital bits of control information contained within the 'request packet.'" *Id.* (emphasis in original). Nowhere in Rambus's appellate briefing did Rambus argue that a read request was *not* part of a request packet. *See generally id.* at *15-*19; Reply Brief for Rambus Inc. as Plaintiff-Appellant, 2002 WL 32817343, *16-*18 (Fed. Cir. Mar. 7, 2002). Instead, Rambus (and as shown above, the specification) consistently referred to the "request" as the command contained in AccessType[0:3], the second through fifth bits of Rambus's preferred embodiment of the request packet.

The Federal Circuit nonetheless construed "read request" more broadly than Rambus proposed. It held that a "read request" was "a series of bits used to request a read of data from a memory device where the request identifies what type of read to perform." *Infinion*, 318 F.3d at 1093. In so doing, the court seems to have rejected the argument that a read request must be contained within a request packet. *Id.* The court quoted two dependent claims from U.S. Patent No. 6,034,918 that recited the need to include a read request and block size information "in a request packet" and then "in the same request packet." *Id.* at 1093.¹¹ The court then criticized the district

¹¹ These claims were not cited to the court in Rambus's appellate briefing. *See generally id.* at *15-*19; Reply Brief for Rambus Inc. as Plaintiff-Appellant, 2002 WL 32817343, *16-*18 (Fed. Cir. Mar. 7, 2002).

1 court's interpretation (and Infineon's) for being irreconcilable with those two claims. *Id.*

2 The Manufacturers acknowledge the *Infineon* decision, but argue that their construction
3 requiring a request to be inside a request packet is consistent with it. The Manufacturers point out
4 that *Infineon* rejects the notion that a request must include address and control information, *id.* at
5 1092, but that *Infineon* does not foreclose the construction they now proffer. The court disagrees.
6 For better or for worse, the *Infineon* decision is quite clear. Its claim differentiation reasoning
7 rejects the Manufacturers' proposed construction requiring that a request be sent in a request packet.
8 The court therefore adheres to the construction of "read request," "write request" and "transaction
9 request" from *Infineon*.

10 2. Additional "Transaction" Terms

11 The parties also dispute the proper construction of various "transaction" terms that were not
12 construed in *Infineon*, but the disputes largely turn on the same issue: whether or not the
13 "transaction" requires the use of a request packet. The parties use the term "operation code" to
14 illustrate their dispute.¹²

15 Rambus construes an operation code as "one or more bits to specify a type of action." The
16 Manufacturers construe operation code as "one or more bits in a request packet used to specify a
17 type of action to be performed." Semantics aside, the substantive difference in the proposed
18 construction is whether an operation code must be sent in a request packet.

19 In prior proceedings, this court construed "operation code" as "one or more bits to specify a
20 type of action," which is now Rambus's proposed construction. *See Hynix I*, 2004 WL 2610012, at
21 *9-*13. The Manufacturers argue that this court erred in relying on the dictionary definition to
22 determine the ordinary meaning of "operation code." The court's analysis did cite the definition of
23 "operation code" contained in *The Authoritative Dictionary of IEEE Standard Terms*. *See id.* at *11
24 (citing *Tex. Digital Sys., Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1202 (Fed. Cir. 2002)).

26 ¹² The other "transaction" terms with similar construction disputes are: block size
27 information, control information, precharge information, address information, read operation, write
28 operation, request for a write operation and set register request.

And had the court stopped there, its prior construction might have run afoul of the Federal Circuit's approach to claim construction. *See Phillips*, 415 F.3d at 1320-23. But the court did not stop with the ordinary meaning conveyed by the dictionary. The court then construed "operation code" in light of various dependent claims that recited the use of the operation code as part of a request packet. *See Hynix I*, 2004 WL 2610012, at *9-*13. To be sure, the court also considered the specification, which states that "the first byte contains two 4 bit fields containing control information, AccessType[0:3], an op code (operation code), which, for example, specifies the type of access[.]" '184 patent, col. 9, ll. 39-41. This demonstrates that AccessType[0:3] – a portion of Rambus's preferred packet embodiment – is an operation code. It does not, however, foreclose the possibility that an operation code could exist outside of a packet. Hence, the specification's ambivalence and the explicit structure of the dependent claims confirm that the phrase "operation code" receives its ordinary meaning and is not limited to being sent as part of a request packet.

The Manufacturers argue that the court should not rely on claim differentiation because Rambus's original claims in 1990 did not include dependent claims explicitly claiming the use of an operation code as part of a request packet, and therefore the current structure of Rambus's claims should be "ignored as a litigation-driven attempt to broaden the scope of the Farmwald patents beyond the scope of the invention set forth in the specifications." The Manufacturers cite no support for this argument. Perhaps the Federal Circuit's concerns about expert testimony – that it is "generated at the time of and for the purpose of litigation and thus can suffer from bias that is not present in intrinsic evidence" – should also reach intrinsic evidence that is generated as litigation occurs. *See Phillips*, 415 F.3d at 1318. On the other hand, the only value of a patent claim is to exclude, and it is naive to think that a patent is prosecuted *without* an eye to litigation. Absent more compelling support, the court cannot accept the Manufacturers' invitation to ignore intrinsic evidence because it might have been "litigation-driven."

It is also worth noting that an "operation code" specifies an action generically. For example, an operation code like AccessType[0:3] specifies a read request, a write request, or certain other possible operations. *See* '184 patent, col. 9, l. 47 - col. 10, l. 14 (explaining additional possible

operations, like control register access, which permits the device's control register to be reprogrammed). In other words, an operation code includes the concepts of a read request or write request. It would be inconsistent with *Infineon* for this court to hold that a read or write request need not be sent in a packet, but that the general family of requests (operation codes) must all be sent in a packet. Accordingly, the court adopts the constructions for the "transaction" terms that do not include a "request packet" limitation, consistent with its claim construction order in *Hynix I* and the reasoning of *Infineon*.

3. "Data"

Claim term:	Rambus's construction:	The Manufacturers' Construction:
"data"	Plain meaning. No construction is necessary. Alternatively, if Court deems construction necessary, "one or more bits representing information."	One or more bits written to/read from the memory array.

Apart from the dispute over importing a "request packet" limitation into various transaction terms, the parties dispute the construction of the term "data" in various limitations dealing with transactions within the memory device. The dispute turns on whether "data" refers to any bit of information, or whether "data" refers only to bits of information written to or read from a memory array. The court previously declined to construe the term "data," *see Hynix I*, 2004 WL 2610012, at *20, and it is not clear why the term must be construed here as no motion for summary judgment of non-infringement or invalidity turns on the construction of the term "data."

The Manufacturers base their argument on the specification's summary of invention, where Rambus describes the invention as ". . . includ[ing] a plurality of bus lines for carrying substantially all address, data, and control information needed by said memory devices . . ." '184 Patent, col. 3, ll. 54-56. The Manufacturers argue from this that Rambus explicitly distinguished "data" information from "address" or "control" information. The Manufacturers claim that Rambus "consistently and repeatedly" made this distinction, though they supply no additional citations to the specification to support this assertion.

CLAIM CONSTRUCTION ORDER FOR THE FARMWALD/HOROWITZ PATENTS AND ORDER DENYING THE MANUFACTURERS' MOTIONS FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND INVALIDITY DEPENDING ON CLAIM CONSTRUCTION — C-05-00334 RMW; C-05-02298-RMW; C-06-00244-RMW

1 Meanwhile, Rambus argues that data does not need construction or should be construed to
2 mean "one or more bits representing information." Rambus emphasizes that in discussing a
3 preferred implementation, the specification describes a protocol for accessing and reprogramming a
4 control register. *See id.*, col. 9, l. 66 - col. 10, l. 14. In that situation, the request packet's
5 AccessType field indicates that the master device seeks access to the control register, the Address
6 field then specifies the address of the control register, and some of the Address field can be used to
7 "represent or include data to be loaded into that control register." *Id.*, col. 10, ll. 6-8. Rambus
8 argues that since a control register is not a memory array, the Manufacturers' definition of "data" is
9 too narrow because the specification describes writing "data" to a control register.

10 It is clear that the specification distinguishes three types of information in the context of the
11 multiplexed bus architecture: address, control and data. Beyond the single example cited by the
12 Manufacturers, the specification makes clear that in a preferred implementation of Rambus's new
13 bus, "8 bus data lines and Addressvalid bus line carry address, data, and control information for
14 memory addresses up to 40 bits wide." *Id.*, col. 4, ll. 2-5. This sentence in the specification shows
15 the impossibility of construing the term "data" outside of the context of the claims. The bus is
16 composed of eight *data* lines that carry three different types of information. Where "data" is used as
17 an adjective to modify a bus line, only Rambus's proposed construction makes sense. But in
18 discussing the types of information carried over the bus's data lines, the specification distinguishes
19 between three kinds: address information, control information, and data information. Where "data"
20 is used as an adjective to modify "information," the Manufacturers' construction makes sense.
21 Finally, the specification refers to writing "data" to a control register. Here, the specification uses
22 "data" as a noun, and the Manufacturers' construction cannot be reconciled with the fact that a
23 control register is not a memory array. As shown, the word "data" takes on differing meanings in
24 the Farmwald/Horowitz specification, and the court does not believe one construction of the term is
25 necessarily appropriate.

26 Accordingly, the court turns to the claims, where the term "data" appears dozens of times.
27 As used in the claims, "data" most often appears as a noun, not as the adjective that often appears in

1 the specification. For example, Claim 14 of the '184 patent uses the term "data" to refer to
2 information to be written to a memory array. *See* '184 patent, col. 25, l. 57 - col. 26, l. 6. The claim
3 covers a method of operating a memory device including "receiving first block size information
4 from a master, wherein the first block size information defines a first amount of *data* to be sampled
5 by the memory device in response to a write request" and "sampling a first portion of the first
6 amount of *data* synchronously." In this method claim, the memory device receives a write request,
7 and the block size information defines the amount of data for the memory device to receive in
8 response to that write request. In response to that information, the memory device then samples the
9 bus to obtain data to write to its memory array. Here, the Manufacturers' construction is the most
10 precise (though Rambus's is still accurate). Similarly, in U.S. Patent 6,715,020, claim 1 recites a
11 controller device featuring "first output driver circuitry to output block size information to the
12 memory device, wherein the block size information defines an amount of data to be output by the
13 memory device[.]" *See* col. 24, ll. 57-65. Here, a controller transmits block size information to the
14 memory device telling the memory device how much data to output. This use of data refers to
15 information to be read from the memory array.

16 On the other hand, U.S. Patent No. 6,314,051's claim 27 demonstrates the shifting contextual
17 uses of the term "data." It recites a memory device that includes "a programmable register to store a
18 value which is representative of a number of clock cycles of the external clock signal to transpire
19 before sampling a first portion of *data*, wherein the first portion of *data* is sampled in response to an
20 operation code" and "*data* input receiver circuitry to sample the first portion of *data* synchronously
21 with respect to the external clock signal." In this claim, "data" appears in both its noun and adjective
22 forms. To be sure, where it is used as a noun, it refers to data to be sampled from the bus after a set
23 time period. Where it modifies "input receiver," however, its meaning seems ambiguous. In the
24 preferred embodiment, the bus is multiplexed and the data lines carry address, data, and control
25 signals to the input receivers. Thus, the input receivers receive more than just data information to be
26 written to the memory array, they also receive address and control information. In this claim, the
27 "data input receiver circuitry" samples data information, but it should not be construed to sample

only data information. Instead, a person of ordinary skill in the art would recognize that "data input receiver circuitry" could sample any type of information from the bus.

That aside, the asserted claims predominantly use the term "data" as a noun and in those contexts, the Manufacturers' construction seems more precise. Accordingly, the court adopts the Manufacturers' construction of "data," namely, as "one or more bits written to/read from the memory array" where the term appears as a noun. The court is mindful, however, that it is being asked to interpret "data" without the context of any invalidity or non-infringement arguments. In the event that this construction of "data" conflicts with the context of a specific claim, the court will revisit the issue.

C. The "Clocking" Terms

The next cluster of disputes between the parties involves the scope of claims related to the clocking features of Rambus's inventions. This dispute influences the construction of "internal clock signal," "external clock signal," "sample" and various additional terms incorporating these. Like the dispute over the "device" and "transaction" terms, the "clocking" terms appear throughout Rambus's claims. Unlike the "device" and "transaction" families of terms, the Federal Circuit has not construed the "clocking" terms. The only prior construction of some of these terms was rendered by this court in *Hynix I*. See 2004 WL 2610012, at *20-*21 (construing "first external clock" and "second external clock"). The dispute largely turns on the extent to which the clocking scheme described in the Farmwald/Horowitz specification limits the scope of Rambus's claims.

1. The Manufacturers' Compliance with the Patent Local Rules

As a preliminary matter, Rambus points out that the Manufacturers' proposed constructions of various clocking terms are not the constructions they proposed in their joint claim construction statement.¹³ Indeed, the Manufacturers' revisions to their constructions of "external clock signal"

¹³ For example, the Manufacturers had previously submitted that an "external clock signal" was "a continuously periodic signal from a source external to the device, which travels along a single bus clock line where the signal is sampled by the device at two separate points along the bus clock line." See, e.g., Joint Claim Construction Statement, C-05-00334-RMW, Appendix A at 15 (N.D. Cal. Jul. 11, 2007). The Manufacturers now argue that an "external clock signal" is properly construed as "a continuously periodic signal, from a source external to the device that provides an early clock and a late

1 and "sample" trickle down and affect their construction of 42 of the 72 disputed terms in this case.
 2 Rambus therefore requests this court to strike the entirety of the Manufacturers' responsive brief on
 3 claim construction. Meanwhile, the Manufacturers claim that they "revised some proposed
 4 constructions . . . in an effort to narrow the issues in dispute and also for clarity."

5 The Patent Local Rules in effect at the time¹⁴ the Manufacturers changed their proposed
 6 claim constructions do not explicitly forbid this shift. *See generally* Patent Local Rule 4, *compare*
 7 *with* Patent Local Rule 3-7 (requiring a showing of good cause and an order of the court to amend or
 8 modify infringement or invalidity contentions). However, such changes in position violate the spirit
 9 of the applicable Rule 4. Rule 4-2 requires the parties to exchange preliminary claim construction
 10 proposals, as well as the basis for those proposals. Rule 4-3 then requires the parties to jointly file a
 11 claim construction and prehearing statement containing a list of agreed-upon constructions, a list of
 12 the parties' proposed claim constructions where they disagree, a disclosure of the evidence
 13 supporting those proposals, and additional information necessary for conducting the claim
 14 construction hearing. Rule 4-4 explicitly closes discovery with respect to claim construction thirty
 15 days after the filing of the joint statement. Rule 4-5 then sets a schedule for filing claim construction
 16 briefs once discovery has closed.

17 While no provision of the Patent Local Rules explicitly forbids a party from shifting its claim
 18 construction position, the rules strongly suggest that a party is not supposed to do so. Rule 4-4 is
 19 designed to permit the parties to conduct discovery in a timely and orderly manner. It therefore
 20 closes discovery with respect to claim construction thirty days after the submission of the joint claim
 21 construction statement. One clear inequity of the Manufacturers' shift in position is that Rambus
 22 was not able to depose the Manufacturers' expert on their new proposed claim constructions prior to
 23 filing its opening and reply briefs.

24 The Northern District's jurisprudence interpreting the Patent Local Rules has been clear

25 _____
 26 clock from which timing information can be derived."

27 ¹⁴ The Patent Local Rules were revised effective March 1, 2008. The rules discussed here
 28 have not significantly changed, though Rule 3-7 regarding amendments is now Rule 3-6.

CLAIM CONSTRUCTION ORDER FOR THE FARMWALD/HOROWITZ PATENTS AND ORDER DENYING THE
 MANUFACTURERS' MOTIONS FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND INVALIDITY DEPENDING
 ON CLAIM CONSTRUCTION — C-05-00334 RMW; C-05-02298-RMW; C-06-00244-RMW

1 regarding their purpose. "The rules are designed to require parties to crystallize their theories of the
 2 case early in the litigation and to adhere to those theories once they have been disclosed." *Nova*
 3 *Measuring Instruments Ltd. v. Nanometrics, Inc.*, 417 F. Supp. 2d 1121, 1123 (N.D. Cal. 2006)
 4 (discussing infringement contentions). In preventing a party from submitting new infringement
 5 contentions after a claim construction ruling, the court explained that "infringement cases would fall
 6 prey to a vexatious shuffling of positions—a kind of legal musical chairs serving no purpose other
 7 than to entertain highly paid lawyers and to thwart the very intention behind the patent local rules."
 8 *Atmel Corp. v. Information Storage Devices Inc.*, 1998 WL 775115, *2 (N.D. Cal. 1998). The court
 9 further noted that the local rules are "designed to prevent the 'shifting sands' approach to claim
 10 construction." *Id.* at *3.

11 In addition to being stymied in discovery, Rambus also lost the opportunity to use their
 12 opening brief to criticize the Manufacturers' new construction of "external clock signal" and
 13 "sample." Indeed, in its opening brief, Rambus pointed out that Manufacturers' original construction
 14 of "external clock signal" used the term "sample," while their construction of "sample" included the
 15 term "external clock signal." Rambus argued that because the Manufacturers' proposed
 16 constructions were circular, they should be rejected. The Manufacturers' revision of their claim
 17 construction proposals to fix this circularity appears opportunistic.

18 The Northern District's jurisprudence does not instruct on how to remedy a shift in claim
 19 construction positions after the parties have filed their joint claim construction statement. The
 20 nearest case on point involved two parties that had agreed not to construe a claim term, thus granting
 21 it a very broad meaning. *Ultratech, Inc. v. Tamarack Scientific Co.*, 2005 WL 856408, *2 (N.D. Cal.
 22 2005). The defendant therefore conceded infringement. *Id.* After securing a summary judgment of
 23 infringement, the patent holder then appears to have argued that the claim term should be construed
 24 more narrowly to avoid the defendant's argument that the claim was invalid based on prior art. *Id.* at
 25 *2-*3. In that case, Magistrate Judge Larson permitted the defendant to submit an expert report
 26 addressing the new claim construction after discovery had closed. *Id.* at *3. The opinion does not
 27 say whether the court later set aside the summary judgment of infringement based on the prior claim

1 construction.

2 Rambus's proposed remedy – striking the Manufacturers' claim construction brief – is too
3 harsh. Nor is the court willing to ignore the Manufacturers' arguments if they help the court to
4 construe the claims in dispute. Yet the Manufacturers' conduct is not conducive to the orderly
5 progress of this case, and the court disapproves of it.

6 2. "External Clock Signal"

7 Claim term:	Rambus's Construction:	The Manufacturers' Construction:
8 "external clock 9 [signal]"	A periodic signal from a source external to the device to provide timing information.	A continuously periodic signal, from a source external to the device that provides an early clock and a late clock from which timing information can be derived.

10
11 Turning to the claim construction dispute, the parties first disagree on the meaning of
12 "external clock signal." The central dispute is whether Rambus's claims are limited to clock signals
13 generated by the clocking scheme disclosed in the specification. The parties also appear to disagree
14 on whether the signal must be continuous.

15 The Manufacturers argue that the specification discloses only one clocking scheme, and that
16 it requires the external clock signal to provide both an "early clock" and a "late clock" signal. *See*
17 '184 Patent, col. 18, l. 62 - col. 19, l. 44. Accurately synchronizing multiple devices in a high speed
18 system is difficult because of the delay caused by the time it takes for the clocking signal to
19 propagate to all of the system's devices. The specification explains that accurate clocking is possible
20 if each device on the bus monitors two bus clock signals and then derives an internal clock from the
21 midpoint of those two signals. *Id.*, col. 18, ll. 63-66. As discussed, the specification discloses two
22 similar methods for doing this: the early and late clocks and the unterminated clock. *See id.*, col. 18,
23 l. 66 - col. 19, l. 13. Rambus contests that the Farmwald/Horowitz specification discloses only one
24 clocking scheme by citing various snatches of the specification's text. The court disagrees. None
25 discloses another clocking scheme. *Accord Hynix I*, 2004 WL 2610012, at *21 (noting the
26 specification's description of only one clocking scheme).

27 Based on the specification containing only one clocking scheme, the Manufacturers argue

1 that the proper construction of "external clock signal" must include both an early clock signal and a
2 late clock signal. The Manufacturers note that the specification emphasizes that "another object of
3 this invention is to provide a clocking scheme to permit high speed clock signals to be sent along the
4 bus with minimal clock skew between devices." '184 Patent, col. 3, ll. 28-30. The specification also
5 trumpets that "the clocking scheme used in this invention has not been used before and in fact would
6 be difficult to implement in backplane buses due to signal degradation caused by connector stubs."
7 *Id.*, col. 3, ll. 8-11. Drs. Farmwald and Horowitz distinguished their clocking scheme from a prior
8 art clocking scheme based on the unusual ramp-shaped waveform used in the prior art, "in contrast
9 to the normal rise-time signals used in the present invention." *Id.*, col. 3, ll. 11-14. The
10 Manufacturers therefore rely on cases like *On Demand Machine* for the proposition that where the
11 specification clearly defines the limits of the invention and the limits are "described as the advantage
12 and distinction of the invention," the specification may narrow the ordinary meaning of a claim. *See*
13 442 F.3d at 1340.

14 Rambus takes issue with the Manufacturers' claim construction for a number of reasons.
15 First, Rambus counters this argument by pointing out that the Farmwald and Horowitz specification
16 contains a number of inventions, and that only some of the claims are directed to the clocking
17 scheme described in the specification. Rambus argues that the court should not construe every claim
18 in its patents that requires an external clock signal to use the novel clocking scheme Rambus
19 invented. Rambus bolsters this argument by submitting that a person of ordinary skill in the art
20 could have implemented other clocking schemes upon reading Rambus's specification. *See* Murphy
21 Reply Decl. ¶ 131. Because a person of ordinary skill in the art could implement other clocking
22 schemes, Rambus argues it would be improper to limit its claims to just the novel loop-back
23 clocking scheme. The Manufacturers do not respond to this argument because it was raised in
24 Rambus's reply (though this was partially caused by the Manufacturers' shift in claim construction
25
26
27
28

proposals).¹⁵

At the two-day claim construction hearing, the parties focused their arguments on two recent Federal Circuit cases dealing with this quandary, *Golight, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327 (Fed. Cir. 2004) and *Akeva L.L.C. v. Adidas-Salomon AG*, 208 Fed. Appx. 861 (Fed. Cir. 2006).¹⁶ In *Golight*, the dispute turned on whether a claim to a searchlight with a means for "rotating" required the searchlight to rotate 360° (the infringer's searchlight rotated about 345°). 355 F.3d at 1329-30. The court emphasized that it saw "no clear definition or disavowal of claim scope in the written description of the '989 patent that would limit claim 11 to horizontal rotation through 360°." *Id.* at 1331. While the specification did list the ability to rotate through 360° as an advantage, it was "but one feature of the invented search light." *Id.* Because a claim does not have to capture every significant or important feature disclosed in the specification, the court held that it would be improper to limit "rotating" to rotating 360°. *Id.* Despite the fact that the specification disclosed only the 360°-rotating preferred embodiment, the "absence of a clear disclaimer of particular subject matter" led the court to broadly interpret "rotating."

¹⁵ Nevertheless, the Manufacturers and Rambus do disagree on the level of ordinary skill in the art that the court must consider when construing the patents. *See Phillips*, 415 F.3d at 1313 ("The inquiry into how a person of ordinary skill in the art understands a claim term provides an objective baseline from which to begin claim interpretation."). Rambus submits that a person of ordinary level of skill in the art possesses a B.S. in electrical engineering and three to five years of experience designing memory devices like DRAMs. Murphy Decl. ¶ 42. The Manufacturers submit that a person of ordinary skill in the art has a bachelors degree in electrical engineering, mechanical engineering, physics, or an equivalent distinction and four to five years of experience in the design of "electromechanical" products or device design generally. McAlexander Decl. ¶ 9. The parties do not expand on these arguments in their supplemental briefs filed after Rambus's reply. Based only on the scant argument, the court agrees with Rambus that the level of ordinary skill in the art at the time the patents-in-suit were originally filed was an electrical engineering degree and experience in the field of memory design specifically. The Manufacturers' conception of the level of ordinary skill is vague and consequently much too broad. It is implausible that an "electromechanical" device designer, which would seem to include people who design everything from cars to blenders, would be "ordinarily skilled" in this art.

¹⁶ Civil Local Rule 3-4(e) prohibits parties from citing an unpublished opinion of another court if that court's rules prohibit citation. The Federal Circuit does not prohibit or restrict parties "from citing nonprecedential dispositions issued *after* January 1, 2007." Fed. Cir. Rule 32.1(c) (emphasis added). The *Akeva* opinion predates January 1, 2007, and should not be considered. Nevertheless, the court will comment on its holding since "an opinion or order which is designated as nonprecedential is one determined by the panel issuing it as not adding significantly to the body of law." Fed. Cir. Rule 32.1(b).

The *Akeva* case involved a patent to shoes with detachable heels. *See* 208 Fed. Appx. at 862-64. The claim language required "a rear sole *secured* below a portion of [the upper part of the shoe]." *Id.* at 863. The alleged infringer argued that "secured" had to be interpreted in light of the specification as not covering shoes that lacked detachable or rotatable heels. *Id.* The Federal Circuit agreed, and distinguished *Golight* because "the detachable sole of the [patent] is not one of several features, it is the primary feature of the invention." *Id.* at 864. The whole point of the invention was to provide extended life, versatility, and better performance by interchanging rear soles. *Id.* In *Golight* on the other hand, there was no disclaimer where the specification described several significant or important features. *Id.*

Reconciling *Akeva* with *Golight*, and taking into account that "an opinion or order which is designated as nonprecedential is one determined by the panel issuing it as not adding significantly to the body of law," it seems that a feature of a single embodiment discussed in the specification should not limit the interpretation of a claim unless it is the sole inventive feature disclosed in the specification. If there are multiple inventive features, the specification must clearly disclaim or disavow subject matter for the specification to limit a claim term's ordinary meaning. Here, the loop-back clocking scheme is but one of many inventions disclosed in the Farmwald/Horowitz specification; indeed, the patent lists seven distinct objectives in its summary. The new clocking scheme is a discrete object of the invention, separate from providing an improved bus architecture and new memory devices. *See* '184 patent, col. 3, ll. 22-48. Under *Golight*, it would be inappropriate to limit every claim reciting an "external clock signal" to Rambus's novel clocking scheme, and unlike *Akeva*, Rambus's specification discloses multiple inventions. The court therefore rejects the Manufacturers' construction.

Rambus's other arguments bolster and confirm this interpretation. Rambus points to a claim it does not assert in these cases. In U.S. Patent No. 6,807,598 (featuring the same Farmwald/Horowitz specification), Rambus claimed a method of operating an integrated circuit device requiring a first external clock signal and a second external clock signal. *See* '598 patent, col. 27, ll. 56-65; *see also Hynix I*, 2004 WL 2610012, at *20-*21 (construing "first external clock" and

1 "second external clock"). Rambus argues that under the Manufacturers' claim construction, this
2 claim would require a first external clock signal comprised of an early clock and a late clock and a
3 second external clock signal comprised of another early clock and another late clock. Rambus notes
4 that such a construction would prevent that claim from covering the preferred embodiment disclosed
5 in the specification due to the plethora of clocks required, while its construction of external clock
6 signal would allow the claim to be reconciled with the "early clock/late clock" embodiment from the
7 specification.

8 Finally, Rambus points out that Hynix has previously agreed with Rambus's construction of
9 "external clock signal." In *Hynix I*, the parties agreed that an "external clock signal" was "a periodic
10 signal from a source external to the device to provide timing information." *Id.* at *20. The parties
11 had disagreed on the construction of "first external clock signal," which Rambus argued should be
12 construed the same as "external clock signal." The court instead construed "first external clock
13 signal" as "a periodic signal received by the memory device from an external source to provide first
14 timing information." *Id.* at *21.

15 Meanwhile, in litigation with Rambus in the District of Delaware, Micron argued that an
16 "external clock signal" was "a periodic signal received by the memory device from an external
17 source to provide first timing information," i.e., Micron advanced this court's construction of "first
18 external clock signal" as its interpretation of "external clock signal." This is not the same
19 construction that Rambus asserts now because Micron's interpretation might imply a need for a
20 *second* external clock signal, but it is different from Micron's current construction.

21 While arguing that they should not be bound by these prior positions, the Manufacturers do
22 not explain why these prior positions were wrong other than to continue to argue that the
23 specification discloses only one clocking scheme and that the claims should be limited to that
24 scheme. Whether Rambus's specification would allow a person of ordinary skill in the art to devise
25 an "external clock signal" other than the early clock/late clock embodiment disclosed in the
26 specification goes to whether Rambus successfully *enabled* its claims that require only an "external
27 clock signal." If in fact a person of ordinary skill in the art could not implement an external clock

1 signal other than the early clock/late clock, Rambus's claims will fail. But if a person of ordinary
2 skill *could* implement other external clocks as Rambus argues, then it would be improper to limit all
3 of Rambus's claims to the novel clocking embodiment disclosed. Doing so would effectively punish
4 Rambus for having disclosed an additional clocking scheme instead of remaining silent and relying
5 on the prior art. It is thus clear from Rambus's claim differentiation argument, the ordinary meaning
6 of the words "external clock signal," and the parties' prior positions that an "external clock signal" is
7 "a periodic signal from a source external to the device to provide timing information."

8 What is unclear is why an "external clock signal" must also be construed to be "continuous."
9 While the Manufacturers propose this construction, their argument is only developed in footnote 30
10 on page 29 of their brief. Rambus only rebuts the argument by suggesting that "continuous" adds
11 "unnecessary verbiage" to the construction of "external clock signal" in footnote 26 on page 19 of its
12 reply brief. Neither side has developed this argument to the extent the court feels comfortable
13 determining whether an "external clock signal" must be continuous. Nor must the court countenance
14 substantive arguments raised only in footnotes. *See SmithKline Beecham Corp. v. Apotex Corp.*, 439
15 F.3d 1312, 1320 (Fed. Cir. 2006). Accordingly, the court will retain the stipulated construction of
16 "external clock signal" from *Hynix I*.

17 iii. "Internal Clock Signal"

18 Claim term:	Rambus's Construction:	The Manufacturers' Construction:
19 "internal clock 20 signal"	A periodic or gated periodic signal generated in a device to provide timing information for internal operation.	An internally created clock signal that is aligned with the midpoint of the early clock and late clock from the external clock signal. ¹⁷

22 The Manufacturers' proposed construction of "internal clock signal" turns on the court's
23 adoption of their construction of "external clock signal" as requiring early and late clock signals.
24 The court has rejected that construction, and therefore the Manufacturers' construction of "internal
25

26 ¹⁷ In the joint claim construction and prehearing statement, the Manufacturers proposed that
27 an "internal clock signal" was "an internally created clock signal that is aligned with the midpoint of the
28 external clock signal as sampled at two separate points along the bus clock line by the device."

1 clock signal" must also fail.

2 Rambus's proposed construction comes from the joint construction of the term in *Hynix I*.
3 See C-00-20905, Docket No. 326, at 3 (N.D. Cal. Sept. 15, 2003). While Rambus amply illustrates
4 why the Manufacturers' construction must fail, Rambus does not explain why the court should adopt
5 its construction. Specifically, Rambus does not explain why an "internal clock signal" may be
6 periodic or "gated periodic." The requirement that a clock signal be periodic comes from the
7 definition of "clock" shared by persons of ordinary skill in the art. See Murphy Reply Decl. ¶ 141
8 (quoting technical dictionaries to define a clock as a "device that generates periodic signals used for
9 synchronization"). Indeed, the parties agreed that an "external clock signal" must be periodic. But
10 Rambus's briefing never explains why a person of ordinary skill in the art would understand that a
11 clock signal could also be "gated periodic." See McAlexander Decl. ¶ 106.

12 On the second day of the claim construction hearing, Rambus's counsel explained that many
13 devices include a gate for blocking the clock signal to conserve energy when the device is not
14 needed.¹⁸ He urged that persons of ordinary skill in the art would recognize that an internal clock
15 signal could also be gated. The Manufacturers do not respond to this argument; indeed, their expert
16 Mr. McAlexander's opinion is limited to pointing out that the specification does not use the word
17 "gated."

18 While the issue of whether an "internal clock signal" can be a gated periodic signal has been
19 addressed only tangentially, the court will adopt Rambus's construction of an "internal clock signal"
20 from *Hynix I* because the Manufacturers have not demonstrated why the prior stipulated construction
21 should not be adopted. Accordingly, the court construes "internal clock signal" to mean "a periodic
22 or gated periodic signal generated in a device to provide timing information for internal operation."

23 The court notes that Rambus's construction of "internal clock signal" does not define its
24 relationship to the "external clock signal." But it appears clear from the specification that a device's

25
26 ¹⁸ A final version of the hearing transcript for the second day is not yet available. The
27 colloquy between the court and Mr. Detre regarding gated periodic clock signals occurred around 10:21
28 AM. In the final version of the hearing transcript, each line of text has a time stamp. Using these time
stamps, one can locate the cited discussion.

internal clock signal must bear some relationship to an external clock signal received by all of the other devices to ensure that the devices remain synchronized. No such clarification of the term "internal clock signal" is required here, however, because the asserted claims all describe the relationship between the external and internal clock signals necessary for each claim. For example, claim 32 of '051 patent requires circuitry "to generate an internal clock signal having a predetermined phase relationship with respect to the external clock signal." U.S. Patent No. 6,314,051, col. 27, ll. 1-4. On the other hand, a few claims may appear ambiguous in this regard. For example, claim 36 of the '8,020 patent requires "a clock alignment circuit to receive the external clock signal" and that "the clock alignment circuit generates an internal clock signal." U.S. Patent No. 6,378,020, col. 28, ll. 35-38; *see also* U.S. Patent No. 6,426,916, col. 28, ll. 19-23. This language may suggest a break in the linkage between the external clock signal and internal clock signal. This ambiguity is dispelled, however, by the proper construction of "clock alignment circuit." *See infra* III-C-7.

4. "Synchronous" Terms

Claim term:	Rambus's Construction:	The Manufacturers' Construction:
"synchronously with respect to"	Having a known timing relationship with respect to.	Having a fixed timing relationship with respect to.
"synchronous memory device"	A memory device that receives an external clock signal which governs the timing of the response to a transaction request.	A memory device that receives an external clock signal.
"synchronize"	Establish a known timing relationship between.	No construction is necessary.

The Manufacturers argue that "synchronously" must be interpreted to mean "having a *fixed* timing relationship," as opposed to a *known* timing relationship, to reflect the limits of the early clock/late clock system disclosed in the Farmwald/Horowitz specification. The Manufacturers' brief does not further elucidate this argument. At the hearing, counsel for Hynix stated that "the

Manufacturers don't dispute Rambus's proposed construction."¹⁹ No one representing Micron, Nanya or Samsung disagreed with this statement or presented arguments in favor of the Manufacturers' proposed construction. Accordingly, the court adopts Rambus's constructions of "synchronously with respect to" and "synchronize."

The parties next dispute the proper construction of "synchronous memory device." Both parties agree that a synchronous memory device receives an external clock signal. Rambus further suggests that a synchronous memory device must allow the external clock signal to govern its transaction requests. The Manufacturers disagree that the term imposes any additional limit.

Hynix and Rambus previously disputed the construction of this phrase in *Hynix I*, and the court construed a "synchronous memory device" as "a memory device that receives an external clock signal which governs the timing of the response to a transaction request." *See id.* at *9. This is the construction that Rambus now proposes. The Manufacturers' briefing is silent as to why their proposed construction of "synchronous memory device" is correct. Rambus points out that it does not make sense to call a memory device "synchronous" simply because it receives an external clock signal — it must *do* something in response to that clock signal to be considered synchronous. Rambus's argument makes common sense. Furthermore, the Manufacturers fail to explain why the court should deviate from its prior construction. Accordingly, the court adopts its prior construction of "synchronous memory device."

5. "Sample" Terms

Claim term:	Rambus's Construction:	The Manufacturers' Construction:
"Sample/samples /sampling"	Plain meaning. No construction necessary. Alternatively, if the court deems construction is required, "ascertain/ascertains/ascertaining at one or more discrete points in time."	Obtain/obtains/obtaining from the bus synchronously with the internal clock signal. ²⁰

¹⁹ The final version of the transcript from the second day of the hearing is not yet available. Mr. Brown's statement conceding this issue occurred at about 11:40 AM.

²⁰ The Manufacturers previously construed "sample" as "obtain from the bus at intervals defined by the internal clock signal."

Rambus submits that the word "sample" as used in the claims is unambiguous and does not require construction. Where a term's ordinary meaning is readily apparent, the court may simply refer to the dictionary to nail down the "widely accepted meaning of commonly understood words." *Phillips*, 415 F.3d at 1314. Nevertheless, where the parties actually dispute the proper construction of a claim term, the court must construe it rather than let an issue of claim interpretation be decided by the jury. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008). Accordingly, the court declines Rambus's request that the court not construe the term "sample."

The term "sample" is ubiquitous in the asserted claims. For example, in claim 14 of the '184 patent, the verb "sample" appears in two limitations. First, "the first block size information defines a first amount of data to be *sampled* by the memory device in response to a write request." Then, the memory device must "*sample*[e] a first portion of the first amount of data synchronously with respect to a first transition of an external clock signal." The claim language reveals the awkwardness of the Manufacturers' construction. Claim 14 requires the memory device to sample synchronously with respect to an *external* clock signal. The Manufacturers' construction would cause the claim to require the memory device to obtain the data synchronously with the *internal* clock signal as well. The Manufacturers explain that any difficulty in reconciling these issues is moot because their construction of internal clock signal explains its relationship to the external clock signal, and therefore it is not a problem for the memory device to obtain data synchronously with respect to both the internal clock and the external clock because the two are related. However, the court has rejected the Manufacturers' construction of internal clock signal, leaving this problem to linger.

Rambus has provided various dictionary definitions of "sample." For example, the 1988 *Standard Dictionary of Electrical and Electronics Terms* defines "sampled data" as "data in which the information content can be ascertained only at discrete intervals of time." The Manufacturers point to nothing in the claims or specification that conflicts with this ordinary meaning. They do urge that their construction of "sample" follows from limiting the scope of the claims to the early

clock/late clock embodiment. As the court has declined to limit the claims to that clocking scheme, the Manufacturers' rationale for their construction of "sample" also fails. Accordingly, the court construes "sample" to mean "to obtain at a discrete point in time," "samples" as "obtains at discrete points in time," and "sampling" as "obtaining at discrete points in time."

6. Input Receiver(s) Circuitry and Output Driver(s) Circuitry

Claim term:	Rambus's Construction:	The Manufacturers' Construction:
"Input receiver(s) circuitry"	An element/circuitry on the device to receive one or more signals from an external source.	A circuit/circuitry on the device to sample one or more signals from the bus synchronously with the internal clock signal of the device.
"Output driver(s) circuitry"	An element/circuitry that outputs information from the device.	A circuit/circuitry on the device to output data to the bus synchronously with the internal clock signal.

The only major difference between the parties' proposed claim constructions is whether the input receivers and output drivers must respond "synchronously with the internal clock signal." To be sure, this dispute also incorporates the parties' dispute regarding the scope of the clocking terms through the word "internal clock signal," which the court resolved above. Because it sheds additional light on the argument regarding "synchronously with respect to the internal clock signal," the court addresses it briefly.

The Manufacturers note that the specification states that "[o]ne important part of the input/output circuitry generates an internal device clock based on early and late bus clocks." '184 Patent, col. 22, ll. 51-52. The specification also states that input receivers and output drivers must "operate as close in time as possible to midway between the two bus clocks." *Id.*, col. 22, ll. 54-56. From this, the Manufacturers argue that the terms "input receiver" and "output driver" must be interpreted to reflect the need for the early and late bus clocks, and that their construction of "internal clock signal" accounts for this requirement. The Manufacturers overlook the context of the discussion containing these quotes. This discussion relates to the need to account for the delay time between the input samplers and output drivers receiving the device's clock signal and their responding by sampling the bus for data or outputting data to the bus. If this delay time is comparable to the frequency of the system, the delay could cause these circuits to miss their

"window" for sending or receiving data. But this need for specialized clocking to compensate for the circuit's delay time is only necessary in very high-speed environments. In slower environments, the circuits' delay times are irrelevant. The Manufacturers' proposed construction overlooks that the proper construction of "input receiver" and "output driver" must account for their use in *any* system, not just high-speed systems.

The claims reflect this distinction. In U.S. Patent no. 6,715,020, Rambus first claims "a controller device [comprising] first output driver circuitry to output block size information to the memory device, . . . ; and input receiver circuitry to receive the amount of data output by the memory device." Col. 24, ll. 57-65. In the tenth claim of the '5,020 patent, Rambus claims "the controller device of claim 1 further including delay locked loop circuitry, coupled to the first output driver circuitry, to generate an internal clock signal, wherein the first output driver circuitry outputs the block size information synchronously with respect to the internal clock signal." *Id.*, col. 25, ll. 29-33. Under the Manufacturers' construction of "output driver," the final limitation of claim 10 requiring the output driver to output data synchronously with respect to the internal clock signal becomes redundant. A person of ordinary skill reading the '5,020 patent would clearly see that "output driver circuitry" should not be construed to require the output of data "synchronously with respect to the internal clock signal" because claim 10 adds that limitation. Claim 9 of the '5,020 patent similarly undermines the Manufacturers' construction of "input receiver circuitry." *See id.*, col. 25, ll. 24-28. Where a synchronous relationship to the internal clock signal is required to compensate for the circuits' delay times, the claims expressly dictate that requirement.

Unlike the Manufacturers' deficient constructions of these terms, Rambus's constructions are straightforward and appear to reflect the ordinary meaning of the terms. The construction of "input receiver" and "output driver" do, however, deviate slightly from Rambus and Hynix's stipulated construction of these terms:

Claim term:	Rambus's Construction Now:	Hynix and Rambus's Construction Then:
-------------	----------------------------	---------------------------------------

"Input receiver(s) circuitry"	An element/circuitry on the device to receive one or more signals from an external source.	Circuitry on the device to receive one or more signals from an external source. <i>See</i> C-00-20905, Docket No. 326, at 4 (N.D. Cal. Sept. 15, 2003).
"Output driver(s) circuitry"	An element/circuitry that outputs information from the device.	Circuitry that outputs information from the device. <i>Id.</i>

Rambus does not explain the significance of broadening the meaning of "input receiver(s) circuitry" or "output driver(s) circuitry" to include an "element" as well as "circuitry." Rambus submits no evidence that an "element" is synonymous with "circuitry," nor does Rambus explain why the construction of these terms should be broadened beyond what it agreed to in *Hynix I*. At the hearing, the court asked, "What's the significance of element/circuitry?" Rambus's counsel responded that "some of the claims use the term output driver and some of the claims use the term output driver circuitry. When it's output driver, we say it's an element. When it's output driver circuitry we say it's circuitry." Rambus's counsel noted that "There's no significant difference in my view."²¹

Because inserting "element" into the construction of these terms does not appear to create any "significant difference," the court adopts the simpler construction of these terms that Rambus and Hynix agreed to in *Hynix I*.

7. Clock Alignment Circuit

Claim term:	Rambus's Construction:	The Manufacturers' Construction:
"Clock alignment circuit"	A circuit for adjusting the timing relationship between a clock signal and another signal.	A circuit in each device that generates an internal clock signal that is aligned with the midpoint of the early clock and late clock from the external clock signal.

Rambus proposes the claim construction stipulated to by Rambus and Hynix previously. *See* C-00-20905, Docket No. 326, at 3 (N.D. Cal. Sept. 15, 2003). The Manufacturers propose a construction to incorporate the early clock/late clock scheme from the specification. Neither side offers any argument on the merits of these proposed constructions outside of their broader arguments about whether the Farmwald/Horowitz patents are limited to the loopback clocking scheme.

²¹ The final version of the transcript from the second day of the hearing is not yet available. Mr. Detre's discussion with the court occurred at about 10:26 AM.

The phrase "clock alignment circuit" does not appear in the specification, and is used in only two of the claims in suit. Claim 32 of the '051 patent recites a memory device that, among other things, includes "a clock alignment circuit coupled to the clock receiver circuitry, to generate an internal clock signal having a predetermined phase relationship with respect to the external clock signal." Claim 36 of the '8,020 patent recites an integrated circuit device that features "a clock alignment circuit to receive the external clock signal" and further requires the clock alignment circuit to "generate[] an internal clock signal." The court has already rejected the Manufacturers' contention that the internal clock signal must result from the midpoint of an early clock signal and a late clock signal. There is no reason now to imply such a limitation here. Instead, the previously stipulated construction accurately reflects the ordinary meaning of a clock alignment circuit. It is a circuit "for adjusting the timing relationship between a clock signal and another signal." In the two claims-in-suit using the phrase, each claim defines the clock signal and the other signal at issue.

Samsung advances a separate argument in the joint claim construction hearing statement's appendix and in a footnote. Samsung argues that the phrase "clock alignment circuit" is a means-plus-function claim and must be restricted to the embodiments disclosed in the specification, effectively limiting these two claims to the early clock/late clock embodiment. *See* 35 U.S.C. § 112, ¶ 6. The claims at issue do not use the term "means" and are therefore presumed to *not* fall under the requirements for means-plus-function claims. *Linear Tech. Corp. v. Impala Linear Corp.*, 379 F.3d 1311, 1319-20 (Fed. Cir. 2004). A "circuit" though is a combination of electrical components for accomplishing a function. *Id.* at 1320. Thus, the term "circuit" can require further definition under section 112, paragraph 6, but "when the structure-connoting term 'circuit' is coupled with a description of the circuit's operation, sufficient structural meaning generally will be conveyed to persons of ordinary skill in the art, and § 112 ¶ 6 presumptively will not apply." *Id.*

In *Linear Technology*, the claim at issue required "a first circuit for monitoring a signal from the output terminal to generate a first feedback signal." *Id.* The court held that the claim language described the circuit's "objective" (monitoring the output terminal's signal) and the circuit's "output" (a feedback signal). *Id.* It therefore held that because the claim recited the "respective circuit's

operation in sufficient detail to suggest structure to persons of ordinary skill in the art," the claim was presumptively not a means-plus-function claim. *Id.* at 1320-21. Here, the word "circuit" is prefaced by "clock alignment" and each claim requires that the clock alignment circuit "generate an internal clock signal." The claims dictate the circuit's objective (to align at least two signals) and its output (an internal clock signal). Accordingly, section 112, paragraph 6 presumptively does not apply. Samsung failed to make any argument to support its interpretation at the hearing and the single footnote in the Manufacturers' brief addressing this point does not explain why "clock alignment circuit" fails to suggest sufficient structure to a person of ordinary skill in the art. Since Samsung has failed to rebut the presumption against reading these claims as means-plus-function claims, the court concludes that the term "clock alignment circuit" does not fall under section 112, paragraph 6.

8. Delay Locked Loop

Claim term:	Rambus's Construction:	The Manufacturers' Construction:
"Delay lock(ed) loop"	Circuitry on the device, including a variable delay line, that uses feedback to adjust the amount of delay of the variable delay line and to generate a signal having a controlled timing relationship relative to another signal.	A circuit in each device that uses fixed and variable delay lines and feedback to align the internal clock signal with the midpoint of the early clock and late clock from the external clock signal.

Like clock alignment circuit, the terms "delay lock loop," "delay locked loop," and "DLL" do not appear in the written description.²² This term does appear, however, in five of the claims-in-suit. In claim 4 of the '446 patent, the delay lock loop "synchronize[s] the output of the first and second portions of the data with the external clock signal." U.S. Patent No. 6,546,446, col. 25, ll. 17-20. The other claims-in-suit require a delay locked loop to "generate an internal clock signal using the external clock signal" or to generate multiple internal clock signals. *See, e.g.*, U.S. Patent No. 6,697,295, col. 28, ll. 13-19 (claim 45); U.S. Patent No. 6,426,916, col. 28, ll. 19-23 (claim 40); U.S.

²² The absence of the phrase "delay locked loop" from the specification is somewhat curious given that Drs. Horowitz and Farmwald testified that they believed that placing a DLL circuit on each DRAM was the best technology for adjusting the delay of a clock signal to minimize clock skew. *See* Tr. 4131:17-4133:14; 5528:20-5531:18.

1 Patent No. 5,915,105, col. 29, ll. 9-15 (claim 34); U.S. Patent No. 6,034,918, col. 27, ll. 26-31 (claim
2 33).

3 Rambus submits the same construction of the term that it and Hynix agreed to in *Hynix I*.
4 See C-00-20905, Docket No. 326, at 3 (N.D. Cal. Sept. 15, 2003). Hynix and the other
5 manufacturers do not explain why the prior stipulated construction is wrong, except for their
6 argument that the specification discloses only an early clock/late clock clocking scheme and that the
7 terms must be construed to reflect such a scheme. As the court has rejected this argument, the
8 Manufacturers do not further explain why their construction should be adopted. Indeed, the
9 Manufacturers' expert, Mr. McAlexander, has retreated at a recent deposition from the
10 Manufacturers' proposed construction in favor of a prior construction of his that lacked a midpoint
11 limitation. See Detre Supp. Decl., Ex. A at 148:11-149:19.

12 But Mr. McAlexander's prior construction is not the one Rambus proposes. Mr.
13 McAlexander previously explained that the ordinary meaning of a "delay locked loop" was "a circuit
14 loop that uses feedback signals to adjust the timing relationship between two signals." *Id.* Both
15 constructions require a circuit to use feedback to create a timing relationship between two signals.
16 The meaningful differences appear to be that Rambus's construction also requires that the circuit
17 contain a variable delay line and that the circuit use the feedback signal to adjust the variable delay
18 line. Neither party submitted any technical dictionaries defining the phrase, nor do the parties'
19 experts' declarations meaningfully explain the basis for either side's construction.

20 The court must give "delay locked loop" its ordinary meaning at the time of the invention,
21 here, 1990. *Phillips*, 415 F.3d at 1313. Prior art patents, whether cited by any patent-in-suit or not,
22 can assist in determining the ordinary meaning of a term. *Arthur A. Collins, Inc. v. Northern*
23 *Telecom Ltd.*, 216 F.3d 1042, 1044-45 (Fed. Cir. 2000). Such patents provide better insight than
24 expert testimony because they cannot be shaped by the pending litigation and were initially written
25 for the person of ordinary skill in the art. The most relevant patent uncovered by the court's search
26 is U.S. Patent No. 4,338,569, issued July 6, 1982, for a "Delay Lock Loop." For the purposes of this
27 discussion, it is significant that the "delay lock loop" describes the need to use a feedback signal to

control a variable or programmable delay device. *See* U.S. Patent No. 4,338,569, col. 2, l. 40 - col. 3, l. 2; *compare with id.*, col. 11, l. 15 - col. 14, l. 19 (every claim recites a "variable delay means" and a "feedback means" for providing an input to the variable delay means).

Based on this prior art description of a delay lock loop and Rambus and Hynix's prior stipulation, the court concludes that Rambus's proposed construction more accurately captures the ordinary meaning of "delay locked loop" to a person of ordinary skill in the art in 1990. The Manufacturers' proposed construction is too narrow. It suffers from focusing solely on the clocking scheme disclosed in the specification. Mr. McAlexander's prior construction is too broad. It encompasses too much by including any and all circuit loops that use feedback. Rambus's construction appears accurate. Accordingly, the court adopts the stipulated construction of "delay locked loop" from *Hynix I*. A delay locked loop as used in the claims means "circuitry on the device, including a variable delay line, that uses feedback to adjust the amount of delay of the variable delay line and to generate a signal having a controlled timing relationship relative to another signal."

D. Other Terms

Rambus requests construction of "coupled to," "precharged automatically" and "automatically precharged." In the parties' joint claim construction hearing statement, the Manufacturers submitted constructions of these terms that differ from Rambus's. The Manufacturers' brief is silent with respect to these terms, despite Rambus raising them in its opening brief. The Manufacturers' expert declares that he has considered the Manufacturers' proposed constructions, and opines that "the Manufacturers' constructions reflect what one skilled in the art would have understood each term to mean in view of the teachings of the Ware Patents-in-Suit." McAlexander Decl. ¶ 44. The "Ware Patents-in-Suit" refer to the other two patents involved in this litigation that arise from a different application, and the court has construed those claims in a separate order. The three terms addressed here that Rambus raised as needing construction only appear in the Farmwald/Horowitz patents. *See* Joint Claim Construction and Prehearing Statement, C-05-00334, Docket No. 254, Appx. A at 4, 8-9 (N.D. Cal. Jul. 11, 2007). The Manufacturers'

expert's declaration, already conclusory, is entitled to no weight based on its failure to discuss the correct patents. Collectively, the Manufacturers' briefing and their expert's declaration fail to explain the basis for disputing these terms with Rambus.

With respect to the precharge terms, the court can discern no difference between "precharged without an additional command" (Rambus's proposal) and "precharg[ed] without additional instruction" (the Manufacturers' proposal). Because the Manufacturers do not explain any difference, the court adopts Rambus's construction of these terms.

For "coupled to," Rambus proposes "electrically (or otherwise) connected to allow the transfer of signals." The Manufacturers propose that no construction is necessary. Rambus provides various dictionary definitions that suggest that "coupled" is synonymous with "connected," and the Oxford English Dictionary agrees, noting that "to couple" may mean "to join or connect in any way." Moreover, "the term coupled is a term of art in patent parlance that means electrically (or otherwise) connected to allow the transfer of signals." *Intel Corp. v. Broadcom Corp.*, 172 F. Supp. 2d 478, 490-91 (D. Del. 2001) (holding that a node "does not as part of its own definition have to be coupled, or electronically connected, to the communication medium"). In light of these definitions, case law, and the Manufacturers' failure to make any contrary argument, the court adopts Rambus's construction. Accordingly, the court construes "coupled to" as "electrically (or otherwise) connected to allow the transfer of signals."

IV. NON-INFRINGEMENT

The Manufacturers have moved for summary judgment of non-infringement contingent on the court's adoption of their proposed constructions of "device," the "transaction" terms, and the "clocking" terms. As the court has declined to adopt the Manufacturers' constructions of those terms, the court denies their motion for summary judgment of non-infringement as moot.

V. INVALIDITY BASED ON WRITTEN DESCRIPTION

Contingent on the court adopting certain claim constructions proposed by Rambus, the Manufacturers move for summary judgment of invalidity. The Manufacturers argue that various claims are invalid for failing to comply with the written description requirement in 35 U.S.C. § 112,

¶ 1 and for failing to claim the subject matter the inventors regarded as their invention under 35 U.S.C. § 112, ¶ 2.

A. The Manufacturers' Burden on Summary Judgment

A patent must contain a written description of the invention. 35 U.S.C. § 112, ¶ 1. This requirement ensures that "the patentee had possession of the claimed invention at the time of the application, i.e., that the patentee invented what is claimed." *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336, 1344-45 (Fed. Cir. 2005). Whether a patent satisfies the written description requirement is a question of fact. *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563 (Fed. Cir. 1991) (reversing summary judgment of invalidity for want of written description because whether drawings adequately described the invention could not be decided as a matter of law). The jury must determine whether a person of ordinary skill in the art would recognize that the inventor possessed the claimed invention. *Id.* at 1563-64. The Manufacturers' burden of persuasion on this question is clear and convincing evidence. *Ralston Purina Co. v. Far-Mar-Co, Inc.*, 772 F.2d 1570, 1574 (Fed. Cir. 1985).

The Federal Circuit has recently explained that "[c]ompliance with the written description requirement is a question of fact but is amenable to summary judgment in cases where no reasonable fact finder could return a verdict for the non-moving party." *PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1307 (Fed. Cir. 2008) (citing *Invitrogen Corp. v. Clontech Labs., Inc.*, 429 F.3d 1052, 1072-73 (Fed. Cir. 2005)). It must be noted that *Invitrogen* involved a motion for partial summary judgment by the *patentee* that its patent complied with the written description requirement, which is not the case here. 429 F.3d at 1072-73. If the *alleged infringer* is challenging the patent's validity, the movant must show that no reasonable jury could conclude that its evidence fails to clearly and convincingly show that the written description requirement has not been met. *Accord Vas-Cath*, 935 F.2d at 1567. Plainly, this is a high burden to meet, though it can be met. *See University Of Rochester v. G.D. Searle & Co., Inc.*, 358 F.3d 916, 927 (Fed. Cir. 2004) (rejecting the argument that "a patent may not be held invalid on its face" on summary judgment).

B. The Written Description Requirement

CLAIM CONSTRUCTION ORDER FOR THE FARMWALD/HOROWITZ PATENTS AND ORDER DENYING THE MANUFACTURERS' MOTIONS FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND INVALIDITY DEPENDING ON CLAIM CONSTRUCTION — C-05-00334 RMW; C-05-02298-RMW; C-06-00244-RMW

1 The Manufacturers move for summary judgment, arguing that the Farmwald/Horowitz
2 specification does not satisfy the written description requirement for any claim featuring a "device"
3 limitation, any of the "transaction" terms, or any of the "clocking" terms.

4 The parties generally agree on the legal framework of this dispute. The parties agree that the
5 Farmwald/Horowitz specification discloses a memory device that uses a narrow, multiplexed bus
6 interface, a packet-based transaction protocol, and a early clock/late clock scheme for synchronizing
7 devices and reducing clock skew. The parties also agree that the Federal Circuit's case law
8 recognizes two situations in which a specification that adequately describes a species might fail to
9 adequately describe a claim to the genus. *See Bilstad v. Wakalopulos*, 386 F.3d 1116, 1125-26 (Fed.
10 Cir. 2004). The first situation applies where the art is too unpredictable for the disclosure of a
11 species to show that a patentee also possessed the genus. *See id.* at 1125 (citing *In re Curtis*, 354
12 F.3d 1347 (Fed. Cir. 2004)). The Manufacturers' motion for summary judgment does not assert this
13 first argument. Reply at 10.

14 The Manufacturers' argument rests on the second scenario described in *Bilstad*. The Federal
15 Circuit has held a claim invalid under the written description requirement where the specification
16 emphasizes the species while disclaiming the genus. *Bilstad*, 386 F.3d at 1126 (citing and
17 explaining *Tronzo v. Biomet, Inc.*, 156 F.3d 1154 (Fed. Cir. 1998)). At this point, the parties
18 disagree about what a patentee must say in the specification to limit the patent's written description
19 to the species disclosed. Rambus relies on the *Bilstad* court's explanation of *Tronzo*. The *Bilstad*
20 court characterized the standard as requiring the patentee to "specifically distinguish" a species from
21 its genus or "expressly disclaim" other species for the written description not to provide support for a
22 claim to a genus. *Id.* at 1125. The "specifically distinguish" language was quoted from *Tronzo*,
23 where the court explained that, "instead of suggesting that [the patent] encompasses additional
24 shapes, the specification specifically distinguishes the prior art as inferior and touts the advantages
25 of the [claimed shape]." 156 F.3d at 1159. Based on this reasoning, the court held that "such
26 statements make clear that [the patent] discloses only [the claimed shape] and nothing broader." *Id.*
27 Accordingly, the written description could not support a claim to a device with a generic shape. *Id.*

1 The Manufacturers disagree with Rambus's characterization that the law requires the
2 specification to "specifically distinguish" or "expressly disclaim" other species. The Manufacturers
3 point out that under *Phillips* a claim may not be interpreted to cover material that the specification
4 "expressly disclaims." See 415 F.3d at 1316 ("In other cases, the specification may reveal an
5 intentional disclaimer, or disavowal, of claim scope . . . In that instance . . . the inventor has
6 dictated the correct claim scope, and the inventor's intention, as expressed in the specification, is
7 regarded as dispositive."). Given *Phillips*' guidance on claim construction, it seems to logically
8 follow that no claim should be invalid for violating the written description requirement as in *Tronzo*
9 because no claim should be construed broadly enough to raise that issue. The Manufacturers argue
10 that this demonstrates that *Tronzo* is broader than the situation of "express disclaimer" because the
11 Federal Circuit could not have meant to conflate the written description requirement and claim
12 construction. The court is not so sure. See *Lizardtech, Inc. v. Earth Resource Mapping, Inc.*, 433
13 F.3d 1373, 1376-78 (Fed. Cir. 2006) (discussing tension between written description and claim
14 construction) (Rader, J., dissenting from denial of rehearing *en banc*). The rule that a specific
15 disclaimer should limit the construction of a claim (and hence avoid a written description problem
16 like the one in *Tronzo*) accords well with the general canon that claims should be construed to
17 preserve their validity. See *Phillips*, 415 F.3d at 1327-28 (discussing the values and limits of the
18 preserve validity canon).

19 Furthermore, the panel opinion in *Lizardtech* demonstrates where *Tronzo* might apply
20 despite *Phillips*' limits on claim construction. In *Lizardtech*, the specification described a single way
21 of accomplishing the claimed computer process. 424 F.3d 1336, 1344 (Fed. Cir. 2005). It also
22 explained the "disfavored" prior art. *Id.* at 1345. Faced with a generic claim to any method of
23 accomplishing the claimed computer process, the court held the claim invalid for failing to satisfy
24 the written description requirement because the specification would not have demonstrated to a
25 person of ordinary skill in the art that Lizardtech possessed the ability to perform the method other
26 than by the disclosed process. *Id.* at 1345-46. This issue only arose, however, because the patent
27 explicitly contained separate claims to Lizardtech's specific, disclosed method and to the generic

1 method. *See id.* at 1343 (comparing the scope of the claims). Because the court could not narrowly
 2 construe the generic claim in the face of the more specific claims, it had to reach the issue of
 3 whether the claim satisfied the written description requirement. In situations where clear claim
 4 differentiation prevents the court from construing a claim to exclude explicitly disclaimed material,
 5 the *Tronzo* rule provides a backstop.

6 Accordingly, the court interprets the *Tronzo* line of the Federal Circuit's written description
 7 case law as invalidating claims to a genus where the written description specifically distinguished its
 8 embodiment from the genus or expressly disclaims other members of the genus. These clear limits
 9 on the *Tronzo* line of authority take into account that *Tronzo* is an outlier in the Federal Circuit's
 10 jurisprudence. The touchstone of the written description requirement is that the specification must
 11 demonstrate to a person of ordinary skill that the patentee possessed what it claimed. *Pandrol USA,*
 12 *LP v. Airboss Ry. Products, Inc.*, 424 F.3d 1161, 1165 (Fed. Cir. 2005). The court in *Lizardtech*
 13 applied the same standard, noting that after reading the specification, a person of ordinary skill
 14 would have only understood Lizardtech as possessing the specific method described. 424 F.3d at
 15 1345. The *Tronzo* decision, however, does not accord with this principle. By suggesting that claims
 16 covering generic shapes did not satisfy the written description requirement because the patentee
 17 specifically distinguished them, it seems inescapable that the patentee *actually did, in fact, possess*
 18 *devices of other shapes.* *See Tronzo*, 156 F.3d at 1159. How else could the patentee have denigrated
 19 the other shapes if it did not possess them? It seems that the patentee simply did not consider the
 20 other shapes its invention. By contrast, the other lines of cases recognized in *Bilstad* – those
 21 involving unpredictable arts – support the thrust of the other written description jurisprudence
 22 because if an art is unpredictable, it is unlikely that the patentee possessed all of the variants within
 23 the art simply because it possessed one of them. Whether a specification like the one in *Tronzo*
 24 should invalidate a claim under the written description requirement or not is beside the point; *Tronzo*
 25 sets forth a principle that has been repeatedly cited by the Federal Circuit. The court points out the
 26 inconsistency between *Tronzo* and other written description cases only to attempt to cabin a
 27 divergent and confusing doctrine and provide structure for this court's review of the Manufacturers'

motion. *Accord University of Rochester v. G.D. Searle & Co., Inc.*, 375 F.3d 1303 (Fed. Cir. 2004) (opinions of Newman, Lourie, Rader, Linn, Dyk, JJ., expressing concerns regarding the written description requirement); *Lizardtech*, 433 F.3d 1373 (opinions of Lourie, Rader, JJ.).

C. The Level of Ordinary Skill

As discussed above, the written description inquiry is made from the perspective of one of ordinary skill in the art. *In re Ruschig*, 379 F.2d 990, 995-96 (C.C.P.A. 1967); *see also Bilsatd*, 386 F.3d at 1126 (vacating with instructions to make findings regarding the level of ordinary skill in the art). Here, the parties dispute the level of ordinary skill in the art. *See supra*, n. 15. For the purposes of conducting claim construction, the court rejected the Manufacturers' proffered level of skill in the art and accepted Rambus's. The court cannot make such credibility determinations with respect to a motion for summary judgment.

The Manufacturers submit that the difference in opinion regarding ordinary skill in the art should not preclude summary judgment. First, the Manufacturers argue that there is no difference between the two sides' proposed levels of skill in the art. The court disagrees, as discussed above. The Manufacturers' definition of the level of skill in the art is markedly lower than Rambus's.

The Manufacturers next contend that any difference is immaterial because Rambus's expert, Robert Murphy, does not explain the significance of any difference in the levels of skill in the art. To be sure, Mr. Murphy's declaration is sparse on testimony, but Mr. Murphy does testify that the person of ordinary skill under Mr. McAlexander's definition "could very well have no experience with memory devices." Murphy Decl. ¶ 47. This lack of experience supports the inference that Mr. McAlexander's person of ordinary skill would lack familiarity with the prior art and fail to recognize well-known alternative ways of implementing the patents' teachings.

Nevertheless, Rambus is wrong to suggest that the Manufacturers' motion for summary judgment must be denied simply because of this difference of opinions. Rambus cites a single case denying a motion for summary judgment of obviousness because the court found a "genuine issue of material fact as to the level of ordinary skill in the art." *Emerson Elec. Co. v. Spartan Tool, LLC*, 223 F. Supp. 2d 856, 913 (N.D. Ohio 2002). Rambus overlooks that the record in that case was

1 riddled with issues of fact that precluded granting summary judgment. *See id.* at 917 (denying
 2 summary judgment "particularly in light of the conflicting evidence concerning the differences
 3 between the prior art and the asserted claims and defendant's failure to present evidence of some
 4 teaching, suggestion or reason to combine the references"). As with all motions for summary
 5 judgment, the court must draw all reasonable inferences in favor of the non-movant. Here, the
 6 parties dispute the level of ordinary skill in the art; therefore, the court must draw an inference in
 7 favor of Rambus's submission. But if the record demonstrates that even a person of Rambus's level
 8 of ordinary skill would not recognize that Drs. Farmwald and Horowitz possessed the claimed
 9 inventions, the court must still grant summary judgment. In that event, the dispute over the level of
 10 ordinary skill in the art ceases to be a dispute of *material* fact and cannot prevent summary
 11 judgment.

12 **D. Claims Using the "Device" Terms**

13 As a preliminary matter, the court observes that the Manufacturers' motion for summary
 14 judgment proceeds by clusters of terms, and not claim by claim. This presentation makes it difficult
 15 for the court to "*separately* analyze whether the 'written description' requirement has been met as to
 16 the subject matter of *each* claim." *Vas-Cath*, 935 F.2d at 1567 (emphasis in original). That aside,
 17 the Manufacturers argue that the specification "expressly disclaimed" or "specifically distinguished"
 18 any claim to a device that lacks the limitations of their proposed construction, i.e., a narrow,
 19 multiplexed bus interface and the absence of a separate device-select line.

20 To begin, the Manufacturers emphasize the first object of the invention, namely, that the
 21 invention uses "*a new bus interface built into semiconductor devices* to support high-speed access to
 22 large blocks of data from a single memory device by an external user of the data, such as a
 23 microprocessor, in an efficient and cost-effective manner." Mot. at 23 (quoting to '184 patent, col. 3,
 24 ll. 22-26) (emphasis in original). Indeed, Rambus concedes that all of the claims-in-suit implement
 25 this objective. *See* Claim Construction Hrg. Tr. 114:7-20 (June 4, 2008). The Manufacturers
 26 therefore argue that Drs. Farmwald and Horowitz disclaimed any coverage of devices that do not use
 27 "a new bus interface." But the phrase "new bus interface" does not encompass or compel the

1 limitations that the Manufacturers suggest. The bus's interface consists of more than device
 2 selection, the number of bus lines, and whether the bus lines are multiplexed. Indeed, those specific
 3 aspects of bus interface technology are described as distinct objects of Dr. Farmwald and Horowitz's
 4 invention. *See* '184 patent, col. 4, ll. 33-40. Furthermore, those aspects of a bus interface are largely
 5 aspects of the *bus* and are not "built into semiconductor devices." On the contrary, one aspect of the
 6 bus interface that is built into the semiconductor device is the use of programmable registers for
 7 controlling access to the bus included in many of the claims-in-suit. *See id.*, col. 21, ll. 28-31.
 8 While this object may distinguish claims that fail to use "a new bus interface," the phrase "new bus
 9 interface" does not require the claimed devices to interface with a narrow, multiplexed bus or to lack
 10 a device-select line.

11 The Manufacturers next point out the following discussion from the summary of the
 12 invention:

13 In the system of this invention, DRAMs and other devices receive address and
 14 control information over the bus and transmit or receive requested data over the same
 15 bus. Each memory device contains only a single bus interface with no other signal
 pins. Other devices that may be included in the system can connect to the bus and
 other non-bus lines, such as input/output lines.

16 *Id.*, col. 4, ll. 10-16. The Manufacturers argue that this passage specifically distinguishes the
 17 invention from claims to a "memory device" with more signal pins than a single bus interface.
 18 Similar language appears in the detailed description of the invention, where the specification states
 19 that "in the preferred implementation, memory devices are provided that have no connections other
 20 than the bus connections described herein and CPUs are provided that use the bus of this invention
 21 as the principal, if not exclusive, connection to memory and to other devices on the bus." *Id.*, col. 6,
 22 ll. 58-63. This reduces the number of pins on the DRAM interface, and the specification points out
 23 that the state-of-the-art DRAM interface requires too many pins. *See id.*, col. 2, ll. 44-50.

24 Nonetheless, the court cannot agree that these passages indicate as a matter of law that the
 25 specification discloses only memory devices that connect solely to a bus that carries device-select
 26 information. *Compare with Tronzo*, 156 F.3d at 1159. Here, the specification described the
 27 preferred memory device as connecting to the bus and nothing else. It "touted" this feature as

1 reducing the number of pins needed on the DRAM, which in turn permits a number of advances.
2 But this language is not as extreme as the disclaimer in *Tronzo*, and *Tronzo* is an extreme case. In
3 *Tronzo*, the patentee "specifically distinguish[ed] the prior art as inferior and tout[ed] the
4 advantages" of the new implant shape. *Id.* Rambus points out, and the court agrees, that the
5 language used here is not so extreme that Drs. Farmwald and Horowitz claimed a species of
6 "memory devices" while disclaiming the genus as a matter of law.

7 The Manufacturers point to a number of other passages of the specification to support their
8 argument that Drs. Farmwald and Horowitz specifically distinguished and disclaimed devices
9 lacking the limitations of the Manufacturers' proposed construction of "device." Those passages do
10 not impose the limitations the Manufacturers want incorporated. For example, the Manufacturers
11 point to the discussion of how "the DRAMs that connect to this bus differ from conventional
12 DRAMs in a number of ways." See '184 patent, col. 4, ll. 21-31. The first way in which the new
13 DRAMs differ is that they use programmable registers to store control information. This passage
14 *supports* the various claims to a memory device with a register; it does not undercut them. The next
15 passage discusses various aspects of the new bus. It says little about the invention's memory or
16 integrated circuit devices, though it does suggest that they do not need device-select lines because
17 such information is sent over the bus. This discussion does not take the form of an "express
18 disclaimer," however. Finally, the Manufacturers quote that "many of these details have been
19 implemented selectively in certain fast memory devices, but never in conjunction with the bus
20 architecture of this invention." *Id.*, col. 22, ll. 62-65. This passage appears in a discussion of Drs.
21 Farmwald and Horowitz's modifications to accessing the columns of a DRAM's memory arrays. The
22 passage does not concern the broader discussion in the specification, and does not disclaim devices
23 that lack an interface to the narrow, multiplexed bus.

24 E. Claims Using the "Transaction" Terms

25 The Manufacturers next move for summary judgment of invalidity on the claims using the
26 "transaction" terms (i.e., all of the claims) by arguing that the specification does not support claims
27 that fail to incorporate the specification's packet-based protocol. This argument consists of a string

1 cite of portions of the specification discussing the packet protocol and a reference to a single
 2 (misplaced) paragraph of Mr. McAlexander's declaration. *See* Mot. at 25; *compare* McAlexander
 3 Decl. ¶ 104 *with* ¶¶ 138-143. Moreover, the Manufacturers agree with Rambus that non-packetized
 4 transfer protocols were known in the art when Drs. Farmwald and Horowitz filed their application.
 5 *See* Reply at 17 & fn. 10. By this court's reading of the written description jurisprudence, the only
 6 way for the Manufacturers to establish that Rambus's disclosure of a species of transfer protocols
 7 (the packet protocol) does not disclose the entire genus of transfer protocols is for the Manufacturers
 8 to show that Rambus disclaimed or distinguished the other existing transfer protocols.

9 The Manufacturers' briefing cites to chunks of the specification. Mot. at 25 (citing the '184
 10 patent at 8:59-62; 8:66-9:4; 9:11-13; 12:45-48; 12:51-55; 13:4-6; 16:34-38; 16:62-65; 20:17-21;
 11 20:32-38; 20:46-49; 21:28-31; and 22:21-23). None of these passages disclaims other transfer
 12 protocols. Instead, these portions of the specification describe the preferred embodiment and how it
 13 uses the packetized transfer protocol. Under *Tronzo* and *Bilstad*, this is insufficient to establish as a
 14 matter of law that non-packetized protocols are not part of the patents' disclosure because the
 15 patentee did not expressly disclaim or distinguish other transfer protocols.

16 **F. Claims Using the "Clocking" Terms**

17 Finally, the Manufacturers move for summary judgment that every claim incorporating a
 18 "clocking" term is invalid under the written description requirement because the court's construction
 19 of those terms does not incorporate the early clock/late clock limitation of the preferred
 20 embodiment. The Manufacturers' arguments largely rehash their claim construction dispute, but a
 21 few points merit further discussion.

22 The Manufacturers first emphasize that one of the objects of the invention is to provide a
 23 novel clocking scheme "to permit high speed clock signals to be sent along the bus with minimal
 24 clock skew between devices." This passage of the specification is not very relevant, however,
 25 because Rambus's various claims are directed at accomplishing different objects of the invention,
 26 and the claims-in-suit are *not* directed at providing a novel clocking scheme to reduce clock skew.
 27 They are directed at providing a new bus interface instead. *Compare* '184 Patent, col. 3, ll. 22-27

1 *with id.*, col. 3, ll. 28-30. As discussed above, it would be inappropriate to limit independent
2 interface claims to the novel clocking scheme simply because Drs. Farmwald and Horowitz also
3 invented a new clocking scheme.

4 The second cited passage of the specification is more apt. Drs. Farmwald and Horowitz did
5 explain that "one important part of the input/output circuitry generates an internal device clock based
6 on early and late bus clocks" and that it is "important" to control clock skew in systems operating at
7 very high frequencies. *See id.*, col. 22, ll. 50-56. To be sure, Drs. Farmwald and Horowitz "touted"
8 the role of their early clock/late clock system in achieving this. But in so doing, they did not
9 distinguish, disclaim, or denigrate other methods of controlling clock skew by generating an internal
10 device clock. Simply "touting" a species is not enough under *Tronzo* to prohibit claims to the genus.
11 Indeed, discussing a "preferred" embodiment necessarily involves "touting" one solution to the
12 problem, but a patentee's description of its invention is not limited to the preferred embodiment. The
13 Federal Circuit's written description case law requires some additional criticism or distinction of the
14 other members of species to invalidate claims covering those members, and that criticism is lacking
15 here. *See Reply* at 19-20.

16 Accordingly, the court denies the Manufacturers' motion for summary judgment of invalidity
17 based on want of written description under *Tronzo*. By this holding, the court does not foreclose
18 further inquiry into the written description support of the various claims in the Farmwald and
19 Horowitz patents including what was known by one skilled in the art at the time the original
20 application was filed. For example, the Manufacturers first raise in their supplemental brief
21 arguments specific to claims reciting a DLL and suggesting that a person of ordinary skill in the art
22 would not recognize from the specification that Drs. Farmwald and Horowitz possessed those
23 claimed inventions. Indeed, Dr. Horowitz testified that a DLL was a "scarier technology than
24 others" and "ooh, expert, only experts touched that technology." Tr. 4380:6-9. He also
25 characterized a DLL as "one of the trickiest circuits on the world." *See Tr.* 4210:5-10. Other DLL
26 patents hint at this complexity. *See U.S. Patent No. 4,338,569* ("Delay Lock Loop"); *U.S. Patent*
27 *No. 5,614,855* ("Delay Locked Loop," assigned to Rambus). However, because this argument was

not properly raised in the Manufacturers' motion, the court does not reach it now.

G. Section 112, Paragraph 2

The Manufacturers also move for summary judgment pursuant to 35 U.S.C. § 112, ¶ 2, which requires claims to set forth "what 'the applicant regards as his invention'" and to be definite. *Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002) (quoting *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1377 (Fed. Cir. 2000)). The Manufacturers argue that a careful study of the specification reveals that Drs. Farmwald and Horowitz did not consider the claims as they are presently construed to be their invention, and that therefore the claims are invalid.

The section 112, paragraph 2 inquiry is tied up in notions of public notice, and therefore, the most probative evidence with respect to this inquiry is the specification. *See Solomon*, 216 F.3d at 1379-80. Because of this public notice focus, inventor testimony has *no* relevance, even though the text of the statute suggests an inquiry into the inventor's subjective knowledge. *Id.* at 1380.²³ As most recently framed by the Federal Circuit, a claim is invalid under section 112, paragraph 2 if "it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention." *Allen Eng'g*, 299 F.3d at 1349. Despite the need to consider the perspective of one of ordinary skill in the art, the case law clearly states that unlike the written description inquiry this issue is a question of law, not fact. *Solomon*, 216 F.3d at 1377.

There is scant case law applying section 112, paragraph 2. Where it has invalidated a claim, the claim contradicted the specification and the patentee "admit[ted] as much." *Allen Eng'g*, 299 F.3d at 1349. This court has interpreted *Allen Engineering* as holding that a claim is invalid if the

²³ Curiously, the central piece of legislative history regarding the codification of the Patent Act says very little about section 112. *See* Senate Report No. 1979, 82d Cong., 2d Sess. (1952). The only comment regarding the provision at issue is: "The clause relating to the claim is made a separate paragraph to emphasize the distinction between the description and the claim or definition, and the language is modified." The committee report does suggest that this provision results from codifying Revised Statute 4888, which required the inventor to "particularly point out and distinctly claim the part, improvement, or combination which he claims as his invention or discovery." It appears that this "requirement" of section 112 may in fact be nothing more than a requirement that a patent application conclude with claims.

claim cannot be logically reconciled with the specification. *TV Interactive Data Corp. v. Microsoft Corp.*, 2004 WL 2823231, *3 (N.D. Cal. Oct. 13, 2004) (White, J.).

Applying this standard, the Manufacturers' motion must fail. The Manufacturers point to nothing in the claims that logically contradicts the specification. Instead, the Manufacturers emphasize that Drs. Farmwald and Horowitz repeatedly referred to "the present invention" in describing certain embodiments. This is insufficient to show a violation of section 112, paragraph 2. Accordingly, the Manufacturers' motion for summary judgment on this ground is denied.

VI. ORDER

For the reasons set forth above, the court construes the claims as described (and as summarized in Appendix 2). The court denies the Manufacturers' motions for summary judgment of non-infringement and invalidity.

DATED: July 10, 2008



RONALD M. WHYTE
United States District Judge

Appendix 1: Information regarding the claims-in-suit.

U.S. Patent No.; Claim No.	Issuance	Defendant	Asserted in <i>Hynix</i> ?	Claim Language ²⁴
6,182,184; 14	1/30/2001	Hynix, Micron, Nanya & Samsung	No.	<p>[A method of operation of a memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:</p> <p>receiving first block size information from a master, wherein the first block size information defines a first amount of data to be sampled by the memory device in response to a write request;</p> <p>receiving a first write request from the master; and</p> <p>sampling a first portion of the first amount of data synchronously with respect to a first transition of an external clock signal and a second portion of the first amount of data synchronously with respect to a second transition of the external clock signal.]</p> <p>wherein the first transition of the external clock signal is a rising edge transition and the second transition of the external clock signal is a falling edge transition.</p>
6,266,285; 1	7/24/2001	Hynix, Micron, Nanya & Samsung	No.	<p>A method of operation in a memory device having a section of memory which includes a plurality of memory cells, the method comprising:</p> <p>receiving a request for a write operation synchronously with respect to an external clock signal; and</p> <p>sampling data, in response to the request for a write operation, after a programmable delay time transpires.</p>

²⁴

Bracketed text indicates that the claim is dependent on a prior claim. The bracketed text represents the prior claim's language that is incorporated in the dependent claim.

United States District Court

For the Northern District of California

6,266,285; 16	7/24/200 1	Hynix, Micron, Nanya & Samsung	No.	<p>[A method of operation in a memory device having a section of memory which includes a plurality of memory cells, the method comprising:</p> <p>receiving an external clock signal;</p> <p>receiving a request for a write operation synchronously with respect to the external clock signal; and</p> <p>sampling data, in response to the request for a write operation, after a programmable number of clock cycles of the external clock signal transpire.]</p> <p>[further including storing a value which is representative of the programmable number of clock cycles of the external clock in a programmable register on the memory device.]</p> <p>further including receiving a set register request, wherein in response to the set register request, the memory device stores the value in the register.</p>
6,314,051; 27	11/6/200 1	Hynix, Micron, Nanya & Samsung	No.	<p>A memory device having a plurality of memory arrays, wherein each memory array includes a plurality of memory cells, the memory device comprising:</p> <p>clock receiver circuitry to receive an external clock signal;</p> <p>a programmable register to store a value which is representative of a number of clock cycles of the external clock signal to transpire before sampling a first portion of data, wherein the first portion of data is sampled in response to an operation code;</p> <p>and data input receiver circuitry to sample the first portion of data synchronously with respect to the external clock signal.</p>
6,314,051; 32	11/6/200 1	Hynix, Micron, Nanya & Samsung	No.	<p>[A memory device having a plurality of memory arrays, wherein each memory array includes a plurality of memory cells, the memory device comprising:</p> <p>clock receiver circuitry to receive an external clock signal;</p> <p>a programmable register to store a value which is representative of a number of clock cycles of the external clock signal to transpire before sampling a first portion of data, wherein the first portion of data is sampled in response to an operation code;</p> <p>and data input receiver circuitry to sample the first portion of data synchronously with respect to the external clock signal]</p> <p>further including a clock alignment circuit coupled to the clock receiver circuitry, to generate an internal clock signal having a predetermined phase relationship with respect to the external clock signal.</p>

CLAIM CONSTRUCTION ORDER FOR THE FARMWALD/HOROWITZ PATENTS AND ORDER DENYING THE MANUFACTURERS' MOTIONS FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND INVALIDITY DEPENDING ON CLAIM CONSTRUCTION — C-05-00334 RMW; C-05-02298-RMW; C-06-00244-RMW

TSF

United States District Court

For the Northern District of California

6,314,051; 43	11/6/200 1	Hynix, Micron, Nanya & Samsung	No.	<p>[A memory device having a plurality of memory arrays, the memory device comprising:</p> <p>first input receiver circuitry to receive an operation code synchronously with respect to an external clock; and</p> <p>second input receiver circuitry to sample data, in response to the operation code, after a predetermined number of clock cycles of the external clock]</p> <p>wherein the memory device is a synchronous dynamic random access memory.</p>
6,546,446; 2	4/8/2003	Hynix, Micron, Nanya & Samsung	No.	<p>[A synchronous; integrated circuit device having a memory array which includes dynamic random access memory cells, wherein the integrated circuit device comprises:</p> <p>a clock receiver to receive an external clock signal;</p> <p>a plurality of sense amplifiers, coupled to the memory array, to sense data from the dynamic random access memory cells; and</p> <p>a plurality of input receivers to sample an operation code synchronously with respect to the external clock signal, the operation code including precharge information, wherein, in response to the precharge information, the plurality of sense amplifiers is automatically precharged after the data is sensed]</p> <p>wherein the operation code specifies a read operation, and wherein the integrated circuit device further includes a plurality of output drivers to output first and second portions of the data in response to the operation code specifying a read operation.</p>

United States District Court

For the Northern District of California

6,546,446; 3	4/8/2003	Hynix, Micron, Nanya & Samsung	No.	<p>[A synchronous; integrated circuit device having a memory array which includes dynamic random access memory cells, wherein the integrated circuit device comprises:</p> <p>a clock receiver to receive an external clock signal;</p> <p>a plurality of sense amplifiers, coupled to the memory array, to sense data from the dynamic random access memory cells; and</p> <p>a plurality of input receivers to sample an operation code synchronously with respect to the external clock signal, the operation code including precharge information, wherein, in response to the precharge information, the plurality of sense amplifiers is automatically precharged after the data is sensed]</p> <p>[wherein the operation code specifies a read operation, and wherein the integrated circuit device further includes a plurality of output drivers to output first and second portions of the data in response to the operation code specifying a read operation]</p> <p>the plurality of output drivers output the first portion of the data synchronously with respect to a rising edge transition of the external clock signal;</p> <p>and the plurality of output drivers output a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.</p>
6,546,446; 4	4/8/2003	Hynix, Micron, Nanya & Samsung	No.	<p>[A synchronous; integrated circuit device having a memory array which includes dynamic random access memory cells, wherein the integrated circuit device comprises:</p> <p>a clock receiver to receive an external clock signal;</p> <p>a plurality of sense amplifiers, coupled to the memory array, to sense data from the dynamic random access memory cells; and</p> <p>a plurality of input receivers to sample an operation code synchronously with respect to the external clock signal, the operation code including precharge information, wherein, in response to the precharge information, the plurality of sense amplifiers is automatically precharged after the data is sensed]</p> <p>[wherein the operation code specifies a read operation, and wherein the integrated circuit device further includes a plurality of output drivers to output first and second portions of the data in response to the operation code specifying a read operation]</p> <p>further including a delay lock loop, coupled to the plurality of output drivers, to synchronize the output of the first and second portions of the data with the external clock signal.</p>

CLAIM CONSTRUCTION ORDER FOR THE FARMWALD/HOROWITZ PATENTS AND ORDER DENYING THE MANUFACTURERS' MOTIONS FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND INVALIDITY DEPENDING ON CLAIM CONSTRUCTION — C-05-00334 RMW; C-05-02298-RMW; C-06-00244-RMW

United States District Court

For the Northern District of California

6,584,037; 1	6/24/200 3	Hynix, Micron, Nanya & Samsung	No.	<p>A method of operation of a synchronous memory device, wherein the memory device includes an array of dynamic random access memory cells, the method of operation of the memory device comprises:</p> <p>receiving an external clock signal;</p> <p>sampling a first operation code synchronously with respect to the external clock signal, wherein the first operation code specifies a write operation; and</p> <p>sampling data after a number of clock cycles of the external clock signal transpire, wherein the data is sampled in response to the first operation code.</p>
6,584,037; 9	6/24/200 3	Hynix, Micron, Nanya & Samsung	No.	<p>[A method of operation of a synchronous memory device, wherein the memory device includes an array of dynamic random access memory cells, the method of operation of the memory device comprises:</p> <p>receiving an external clock signal;</p> <p>sampling a first operation code synchronously with respect to the external clock signal, wherein the first operation code specifies a write operation; and</p> <p>sampling data after a number of clock cycles of the external clock signal transpire, wherein the data is sampled in response to the first operation code]</p> <p>further including:</p> <p>sampling a second operation code synchronously with respect to the external clock signal, wherein the second operation code specifies a read operation;</p> <p>generating an internal clock signal to synchronize outputting data with the external clock signal, wherein the internal clock signal has a controlled delay time with respect to the external clock signal, wherein the delay time of the internal clock signal is controlled based on a comparison between the internal clock signal and the external clock signal;</p> <p>and outputting data read in response to the second operation code, wherein:</p> <p>a first portion of the data read is output in response to a rising edge transition of the external clock signal; and</p> <p>a second portion of the data read is output in response to a falling edge transition of the external clock signal.</p>

United States District Court

For the Northern District of California

6,584,037; 34	6/24/200 3	Hynix, Micron, Nanya & Samsung	No.	<p>A method of operation of a synchronous dynamic random access memory device, wherein the method comprises:</p> <p>sampling an operation code synchronously with respect to an external clock signal, wherein the operation code specifies that the memory device sample data to be written into a plurality of dynamic memory cells, and wherein the operation code further specifies that the memory device precharge a plurality of sense amplifiers;</p> <p>sampling the data, in response to the operation code, after a delay time transpires;</p> <p>sampling address information to identify a subset of the plurality of dynamic memory cells;</p> <p>writing the data to the subset of the plurality of dynamic memory cells using the plurality of sense amplifiers; and</p> <p>precharging the plurality of sense amplifiers in response to the operation code, wherein the plurality of sense amplifiers is precharged automatically after the data is written.</p>
6,697,295; 45	2/24/200 4	Hynix, Micron, Nanya & Samsung	No.	<p>[A synchronous memory device including an array of memory cells, the synchronous memory device comprising:</p> <p>a clock receiver to receive an external clock signal;</p> <p>a plurality of input receivers to sample a first operation code synchronously with respect to a transition of the external clock signal; and</p> <p>a programmable register to store a binary value that is representative of control information, wherein the memory device stores the binary value in the programmable register in response to the first operation code]</p> <p>[further including a delay locked loop, coupled to the clock receiver, to generate an internal clock signal using the external clock signal]</p> <p>[further including a plurality of output drivers, coupled to the delay locked loop, to output data in response to the internal clock signal, wherein the data is accessed from the memory array]</p> <p>wherein the plurality of output drivers output a first portion of the data synchronously with respect to a rising edge transition of the external clock signal, and wherein the plurality of output drivers output a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.</p>

United States District Court

For the Northern District of California

6,715,020; 1	3/30/200 4	Hynix, Micron, Nanya & Samsung	No.	A controller device for controlling a synchronous dynamic random access memory device, the controller device comprises: first output driver circuitry to output block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device; and input receiver circuitry to receive the amount of data output by the memory device.
6,715,020; 2	3/30/200 4	Hynix, Micron, Nanya & Samsung	No.	[A controller device for controlling a synchronous dynamic random access memory device, the controller device comprises: first output driver circuitry to output block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device; and input receiver circuitry to receive the amount of data output by the memory device] further including second output driver circuitry to output an operation code to the memory device, wherein the operation code specifies a read operation, and wherein, in response to the operation code, the memory device outputs the amount of data.
6,715,020; 14	3/30/200 4	Hynix, Micron, Nanya & Samsung	No.	[A controller device for controlling a synchronous dynamic random access memory device, the controller device comprises: first output driver circuitry to output block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device; and input receiver circuitry to receive the amount of data output by the memory device] wherein the input receiver circuitry samples: a first portion of the amount of data during a first half of a clock cycle of an external clock signal; and a second portion of the amount of data during a second half of the clock cycle of the external clock signal.

United States District Court

For the Northern District of California

6,751,696; 4	6/15/200 4	Hynix, Micron, Nanya & Samsung	No.	<p>[A synchronous memory device including an array of memory cells, the synchronous memory device comprises:</p> <p>clock receiver circuitry to receive an external clock signal;</p> <p>input receiver circuitry to sample a first operation code in response to a rising edge transition of the external clock signal;</p> <p>a programmable register to store a value which is representative of an amount of time to transpire before the memory device outputs data, wherein the memory device stores the value in the programmable register in response to the first operation code; and</p> <p>output driver circuitry to output data in response to a second operation code, wherein the data is output after the amount of time transpires, and wherein:</p> <p>the output driver circuitry outputs a first portion of the data synchronously with respect to a rising edge transition of the external clock signal and outputs a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.]</p> <p>wherein the memory device is a synchronous dynamic random access memory.</p>
6,324,120; 33	11/27/20 01	Nanya & Samsung	Yes.	<p>[A synchronous dynamic random access memory device having at least one memory section including a plurality of memory cells, the memory device comprising:</p> <p>clock receiver circuitry to receive an external clock signal;</p> <p>input receiver circuitry, including a first plurality of input receivers to sample block size information synchronously with respect to the external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a first operation code; and</p> <p>a plurality of output drivers to output the amount of data in response to the first operation code]</p> <p>[wherein the input receiver circuitry samples the first operation code synchronously with respect to the external clock signal]</p> <p>wherein the first operation code includes precharge information.</p>

United States District Court

For the Northern District of California

6,378,020; 32	4/23/200 2	Nanya & Samsung	Yes.	<p>[An integrated circuit device comprising:</p> <p>input receiver circuitry to sample an operation code synchronously with respect to a first transition of an external clock signal, the operation code specifying a read operation; and</p> <p>output driver circuitry to output data in response to the operation code, wherein:</p> <p>the output driver circuitry outputs a first portion of data in response to a rising edge transition of the external clock signal; and</p> <p>the output driver circuitry outputs a second portion of data in response to a falling edge transition of the external clock signal]</p> <p>[further including a memory array having a plurality of memory cells]</p> <p>wherein the input receiver circuitry receives address information synchronously with respect to the external clock signal</p>
6,378,020; 36	4/23/200 2	Nanya & Samsung	Yes.	<p>[An integrated circuit device comprising:</p> <p>input receiver circuitry to sample an operation code synchronously with respect to a first transition of an external clock signal, the operation code specifying a read operation; and</p> <p>output driver circuitry to output data in response to the operation code, wherein:</p> <p>the output driver circuitry outputs a first portion of data in response to a rising edge transition of the external clock signal; and</p> <p>the output driver circuitry outputs a second portion of data in response to a falling edge transition of the external clock signal]</p> <p>[further including a clock alignment circuit to receive the external clock signal]</p> <p>wherein the clock alignment circuit generates an internal clock signal, and the output driver circuitry outputs data in response to the internal clock signal</p>

United States District Court

For the Northern District of California

6,426,916; 9	7/30/200 2	Nanya & Samsung	Yes.	<p>[A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells, the method of operation of the memory device comprises:</p> <p>receiving a value that is representative of a number of cycles of an external clock signal to transpire after which the memory device responds to a first operation code;</p> <p>receiving block size information, wherein the block size information is representative of an amount of data to be output by the memory device in response to the first operation code;</p> <p>sampling the first operation code synchronously with respect to a transition of the external clock signal; and</p> <p>outputting the amount of data, in response to the first operation code, after the number of clock cycles of the external clock signal transpire]</p> <p>wherein the first operation code includes precharge information</p>
6,426,916; 28	7/30/200 2	Nanya & Samsung	Yes.	<p>[A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:</p> <p>clock receiver circuitry to receive an external clock signal;</p> <p>first input receiver circuitry to sample block size information synchronously with respect to the external clock signal, wherein the block size information is representative of an amount of data to be output by the memory device in response to a first operation code;</p> <p>a register which stores a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data; and</p> <p>a plurality of output drivers to output the amount of data in response to the first operation code and after the amount of time transpires]</p> <p>wherein in response to a second operation code, the value is stored in the register</p>

United States District Court

For the Northern District of California

6,426,916; 40	7/30/200 2	Nanya & Samsung	Yes.	<p>[A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:</p> <p>clock receiver circuitry to receive an external clock signal;</p> <p>first input receiver circuitry to sample block size information synchronously with respect to the external clock signal, wherein the block size information is representative of an amount of data to be output by the memory device in response to a first operation code;</p> <p>a register which stores a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data; and</p> <p>a plurality of output drivers to output the amount of data in response to the first operation code and after the amount of time transpires]</p> <p>further including delay lock loop circuitry, coupled to the clock receiver circuitry, to generate an internal clock signal, wherein the plurality of output drivers output the amount of data in response to the internal clock signal.</p>
6,452,863; 16	9/17/200 2	Nanya & Samsung	Yes.	<p>[A method of operation in a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:</p> <p>receiving first block size information from a memory controller, wherein the memory device is capable of processing the first block size information, wherein the first block size information represents a first amount of data to be input by the memory device in response to an operation code;</p> <p>receiving the operation code, from the memory controller, synchronously with respect to an external clock signal; and</p> <p>inputting the first amount of data in response to the operation code]</p> <p>[wherein inputting the first amount of data includes receiving the first amount of data synchronously with respect to the external clock signal]</p> <p>wherein the first amount of data is sampled over a plurality of clock cycles of the external clock signal.</p>

United States District Court

For the Northern District of California

1	6,038,195; 1	3/14/200 0	Samsung	No.	A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:
2					
3					
4					clock receiver circuitry to receive an external clock signal;
5					a register which stores a value which is representative of a delay time after which the memory device responds to a read request;
6					and
7					a plurality of output drivers to output data after the delay time transpires and synchronously with respect to the external clock signal.
8					
9	5,915,105; 34	6/22/199 9	Samsung	Yes.	[A synchronous memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
10					
11					internal clock generation circuitry to generate a first internal clock signal and a second internal clock signal, wherein the internal clock generation circuit generates the first and second internal clock signals using at least a first external clock;
12					
13					an output driver, coupled to the internal clock generation circuitry, the output driver outputs data on a bus in response to the first and second internal clock signals and synchronously with respect to at least the first external clock signal]
14					
15					further including clock receiver circuitry to receive the first external clock and wherein the internal clock generation circuitry includes delay locked loop circuitry, coupled to the clock receiver circuitry, to generate the first internal clock signal and the second internal clock signal using at least the first external clock
16					
17					
18					
19					
20					
21					
22					
23					
24					
25					
26					
27					
28					

United States District Court

For the Northern District of California

6,034,918; 24	3/7/2000	Samsung	Yes.	<p>[A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:</p> <p>receiving an external clock signal;</p> <p>receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request;</p> <p>receiving a first request from the bus controller; and</p> <p>outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal]</p> <p>further including storing a delay time code in an access time register, the delay time code being representative of a number of clock cycles to transpire before data is output onto the bus after receipt of a read request and wherein the first amount of data corresponding to the first block size information is output in accordance with the delay time code</p>
6,034,918; 33	3/7/2000	Samsung	Yes.	<p>[A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:</p> <p>receiving an external clock signal;</p> <p>receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request;</p> <p>receiving a first request from the bus controller; and</p> <p>outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal]</p> <p>further including generating at least one internal clock signal using a delay locked loop and the external clock signal wherein the first amount of data corresponding to the first block size information is output onto the bus synchronously with respect to at least one internal clock signal</p>

Appendix 2: The court's claim constructions.

Claim term:	Construction:
"address information"	One or more bits that indicate a storage location.
"automatically precharged"	Precharged without an additional command.
"block size information"	Information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request
"bus"	A set of signal lines to which a number of devices are connected, and over which information is transferred between devices.
"clock alignment circuit"	A circuit for adjusting the timing relationship between a clock signal and another signal.
"control information"	Information used to control operation.
"coupled to"	Electrically (or otherwise) connected to allow the transfer of signals.
"data"	One or more bits written to/read from the memory array.
"delay lock(ed) loop"	Circuitry on the device, including a variable delay line, that uses feedback to adjust the amount of delay of the variable delay line and to generate a signal having a controlled timing relationship relative to another signal.
"device"	[No separate construction.]
"external clock signal"	A periodic signal from a source external to the device to provide timing information.
"input receiver(s) circuitry"	Circuitry on the device to receive one or more signals from an external source.
"integrated circuit device"	A circuit constructed on a single monolithic substrate, commonly called a 'chip.'
"internal clock signal"	A periodic or gated periodic signal generated in a device to provide timing information for internal operation.
"memory device"	A device in which information can be stored and retrieved electronically.
"operation code"	One or more bits to specify a type of action.
"output driver(s) circuitry"	Circuitry that outputs information from the device.
"precharge information"	One or more bits indicating whether the sense amplifiers and/or bits lines (or a portion of the sense amplifiers and/or bits lines) should be precharged.
"precharged automatically"	Precharged without an additional command.

"read request"	A series of bits used to request a read of data from a memory device where the request identifies what type of read to perform.
"read operation"	Reading data from the memory array as specified in the read request.
"request for a write operation"	A series of bits used to request a write of data to a memory device where the request identifies what type of write to perform.
"sample / samples / sampling"	To obtain at a discrete point in time; obtains at discrete points in time; and obtaining at discrete points in time."
"set register request"	One or more bits to specify that a value be stored in a programmable register.
"synchronize"	Establish a known timing relationship between.
"synchronous memory device"	A memory device that receives an external clock signal which governs the timing of the response to a transaction request.
"synchronously with respect to"	Having a known timing relationship with respect to.
"transaction request"	A series of bits used to request performance of a transaction with a memory device.
"write request"	A series of bits used to request a write of data to a memory device.
"write operation"	Writing data to the memory array as specified in the write request.

Notice of this document has been electronically sent to:

Counsel for Rambus Inc., all actions		Counsel for Hynix entities, C-00-20905 and C-05-00334	
Burton Alexander Gross	Burton.Gross@mto.com	Allen Ruby	ruby@allenrubylaw.com
Carolyn Hoecker Luedtke	carolyn.luedtke@mto.com	Belinda Martinez Vega	bvega@omm.com
Catherine Rajwani	crajwani@sidley.com	Daniel J. Furniss	djfurniss@townsend.com
Craig N. Tolliver	ctolliver@mckoolsmith.com	Geoffrey Hurndall Yost	gyost@thelenreid.com
David C. Yang	david.yang@mto.com	Jordan Trent Jones	jtjones@townsend.com
Douglas A. Cawley	dcawley@mckoolsmith.com	Joseph A. Greco	jagreco@townsend.com
Erin C. Dougherty	erin.dougherty@mto.com	Kenneth Lee Nissly	kennissly@thelenreid.com
Gregory P. Stone	gregory.stone@mto.com	Kenneth Ryan O'Rourke	korourke@omm.com
Jennifer Lynn Polse	jen.polse@mto.com	Patrick Lynch	plynch@omm.com
Keith Rhoderic Dhu Hamilton, II	keith.hamilton@mto.com	Susan Gregory VanKeulen	svankeulen@thelenreid.com
Kelly Max Klaus	kelly.klaus@mto.com	Theodore G. Brown, III	tgbrown@townsend.com
Miriam Kim	Miriam.Kim@mto.com	Tomomi Katherine Harkey	tharkey@thelen.com
Peter A. Detre	detrepa@mto.com	Counsel for Micron entities, C-06-00244	
Pierre J. Hubert	phubert@mckoolsmith.com	Aaron Bennett Craig	aaroncraig@quinnemanuel.com
Rosemarie Theresa Ring	rose.ring@mto.com	David J. Ruderman	davidruderman@quinnemanuel.com
Scott L Cole	scole@mckoolsmith.com	Harold Avrum Barza	halbarza@quinnemanuel.com
Scott W. Hejny	shejny@sidley.com	Jared Bobrow	jared.bobrow@weil.com
Sean Eskovitz	sean.eskovitz@mto.com	John D Beynon	john.beynon@weil.com
Steven McCall Perry	steven.perry@mto.com	Leeron Kalay	leeron.kalay@weil.com
Thomas N Tarnay	ttarnay@sidley.com	Linda Jane Brewer	lindabrewer@quinnemanuel.com
William Hans Baumgartner, Jr	wbaumgartner@sidley.com	Rachael Lynn Ballard McCracken	rachaelmccracken@quinnemanuel.com
		Robert Jason Becher	robertbecher@quinnemanuel.com
		Yonaton M Rosenzweig	yonirosenzweig@quinnemanuel.com

CLAIM CONSTRUCTION ORDER FOR THE FARMWALD/HOROWITZ PATENTS AND ORDER DENYING THE MANUFACTURERS' MOTIONS FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND INVALIDITY DEPENDING ON CLAIM CONSTRUCTION — C-05-00334 RMW; C-05-02298-RMW; C-06-00244-RMW

TSF

Counsel for Nanya entities, C-05-00334		Counsel for Samsung entities, C-05-00334 and C-05-02298	
Chester Wren-Ming Day	cday@orrick.com	Ana Elena Kadala	anita.kadala@weil.com
Craig R. Kaufman	ckaufman@orrick.com	Claire Elise Goldstein	claire.goldstein@weil.com
Jan Ellen Ellard	jellard@orrick.com	David J. Healey	david.healey@weil.com
Jason Sheffield Angell	jangell@orrick.com	Edward Robert Reines	Edward.Reines@weil.com
Kaiwen Tseng	ktseng@orrick.com	Matthew D. Powers	matthew.powers@weil.com
Mark Shean	mshean@orrick.com		
Robert E. Freitas	rfreitas@orrick.com		
Vickie L. Feeman	vfeeman@orrick.com		

Counsel for intervenor, Texas Instruments, Inc., C-05-00334	
Kelli A. Crouch	kcrouch@jonesday.com
Counsel for intervenor, United States Department of Justice, C-00-20905	
Eugene S. Litvinoff	eugene.litvinoff@usdoj.gov
May Lee Heye	may.hey@usdoj.gov
Nathanael M. Cousins	nat.cousins@usdoj.gov
Niall Edmund Lynch	Niall.Lynch@USDOJ.GOV
Counsel for intervenor, Elpida Memory, Inc., C-00-20905 and C-05-00334	
Eric R. Lamison	elamison@kirkland.com
John J. Feldhaus	jfeldhaus@foley.com

Counsel are responsible for distributing copies of this document to co-counsel that have not registered for e-filing under the court's CM/ECF program in each action.

Dated: 7/10/2008

TSF
Chambers of Judge Whyte